

Compal Confidential

VIWG3/VIWG4 DIS M/B Schematics Document

Intel Haswell Processor with DDRIII + Lynx Point PCH

nVIDIA N14X

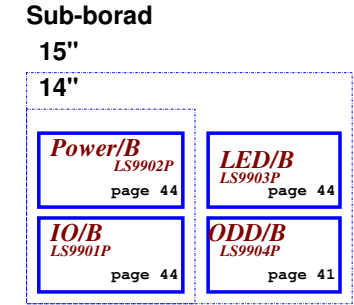
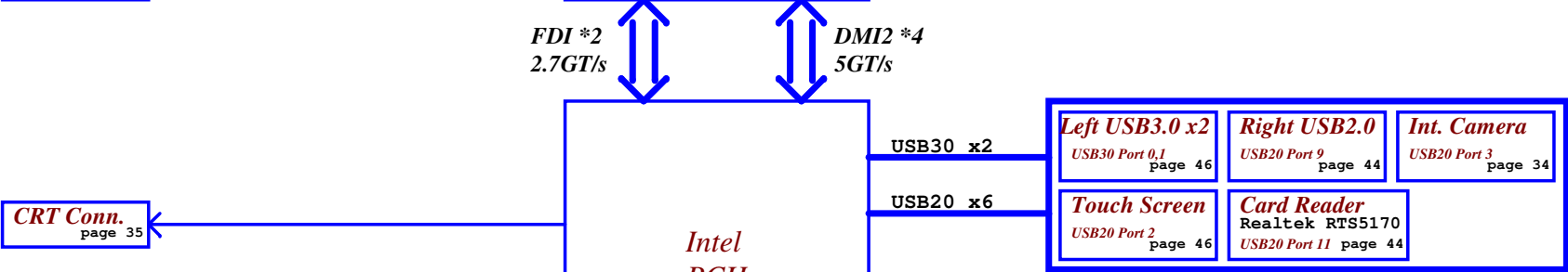
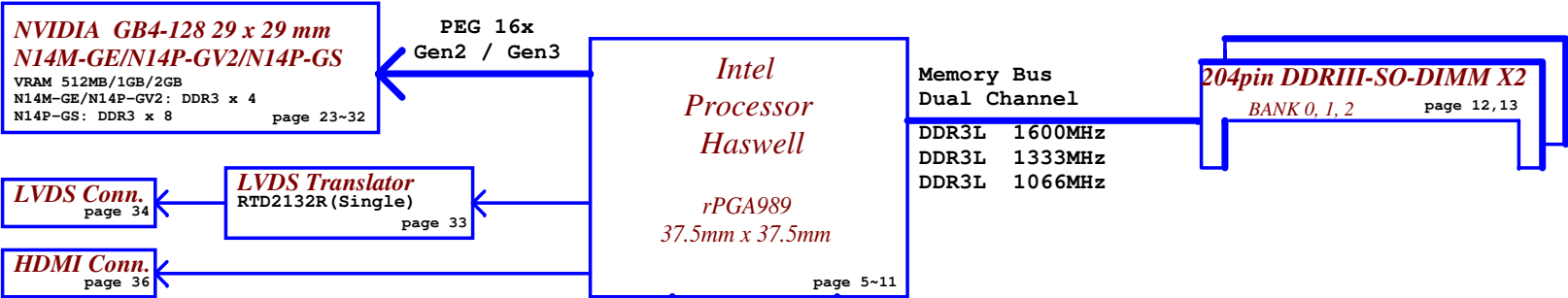
LA-A191P

2013-01-16

REV: 0.1

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Shark Bay



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Voltage Rails

power plane	State	+B	+5VALW +3VALW	+1.35V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.675VS +1.05VS
S0		○	○	○	○
S3		○	○	○	✗
S5 S4/AC		○	○	✗	✗
S5 S4/ Battery only		○	✗	✗	✗
S5 S4/AC & Battery don't exist		✗	✗	✗	✗

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor	1001 100xb

PCH SM Bus address

Device	Address
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 010Xb
LVDS Translator	

NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	✗	✓	✗	✗	✗	✗	✗
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	✓	✗	✗	✗	✗	✗	✓
SMB_EC_DA2	+3VALW	+3VS_VGA						+3VS
SMBCLK	PCH	✗	✗	✗	✓	✓	✗	✗
SMBDATA	+3VALW				+3VS	+3VS		
SML0CLK	PCH	✗	✗	✗	✗	✗	✗	✗
SML0DATA	+3VALW							
SML1CLK	PCH	✓	✗	✓	✗	✗	✓	✗
SML1DATA	+3VALW	+3VS_VGA		+3VS			+3VS	

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID table for AD channel

Vcc	3.3V					
Ra	100K +/- 1%					
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD	
0	0	0 V	0 V	0.300 V	0x00 - 0x0B	MP
1	12K +/- 1%	0.347 V	0.354 V	0.360 V	0x0C - 0x1C	PVT
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26	DVT
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30	EVT

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	USB Port (Left Side) USB3.0
		1	USB Port (Left Side) USB3.0
		2	Touch Screen
	UHCI1	3	USB Camera
		4	
		5	
EHCI2	UHCI3	6	
		7	
		8	
	UHCI4	9	USB/B (Right Side USB2.0)
		10	Mini Card(WLAN)
		11	Card Reader
		12	
	UHCI6	13	

BOM Structure Table

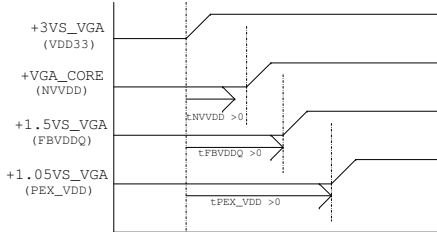
BTO Item	BOM Structure
45 LEVEL	45@
Connector	ME@
For VILG2 (14")	14@
For VILG1 (15")	15@
GPU:N14M-GE	N14@
HDMI	HDMI@
Camera	CMOS@
LAN LDO Mode	LDO@
LAN Switch mode	SWR@
10/100 LAN(AR8162L)	8162@
10/100 LAN(QCA8172)	8172@
N14M-GE SKU	GE@
N14P-GS SKU	GS@
N14P-GV2 SKU	GV2@
N14P-GV2&N14P-GS SKU	GVGS@
Green clock(DIS sku)	GCLK304@
Green clock(UMA sku)	GCLK244@
Green clk support	GCLK@
No Green clk support	NOGCLK@
Nvidia GC6 state	GC6@
Touch Screen SKU	TS@
Optimus SKU	OPT@
UMA SKU	UMA@
VRAM(1000MHz)	1000M@
VRAM(900MHz)	900M@
Unpop	@
Deep S3	DS3@
NO Deep S3	NODS3@
Share ROM	SROM@
Non Share ROM	NOSROM@

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N14x GPIO Pin Definition Table

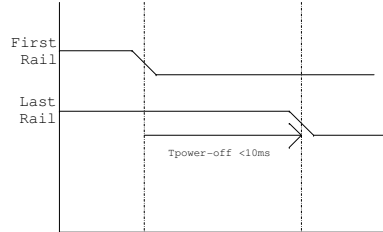
Pin Name	Normal Function	I/O	Functional Description	Default PU/PD
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor	
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM VID:Strap to boot FBVDD/Q
GPIO2-4	Non-support for LCD	O	Panel	100k PD
GPIO5	Reserve			
GPIO6	FB_CLAMP_TGL_REQ	O	Active low FB Clamp toggle request	
GPIO7	3DVision	O	3D Vision L/R signal	100k PD
GPIO8	OVERT	IO	Active Low Thermal Catastrophic Over Temperature	100k PU
GPIO9	ALERT	IO	Active Low Thermal Alert	100k PU
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100k PD
GPIO11	PWM_VID	O	GPU Core VDD PWM control supply overdraw input	
GPIO12	PWR_LEVEL	I	AC power detect or control signal	100k PU
GPIO13	PSI	O	Phase Shedding	PSI:100k PU to enable two phase
GPIO14-19	Non-support for HDA	I	Hot Plug	
GPIO20-21	Reserve			

GPU Power On



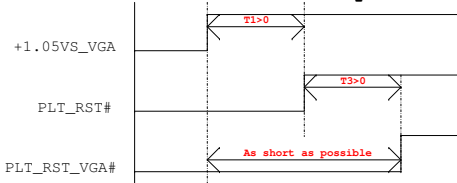
1. all power rail ramp up time should be larger than 40us
2. The total time for all rails to ramp should be within 6ms.
3. A power rail has to ramp up 90% before the next power rail in sequence can start ramping up.
4. No signal should be applied to the GPU before the power rail are fully ramped.

GPU Power Down

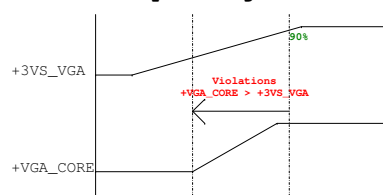


1. All GPU power rails should be turned off within 10ms

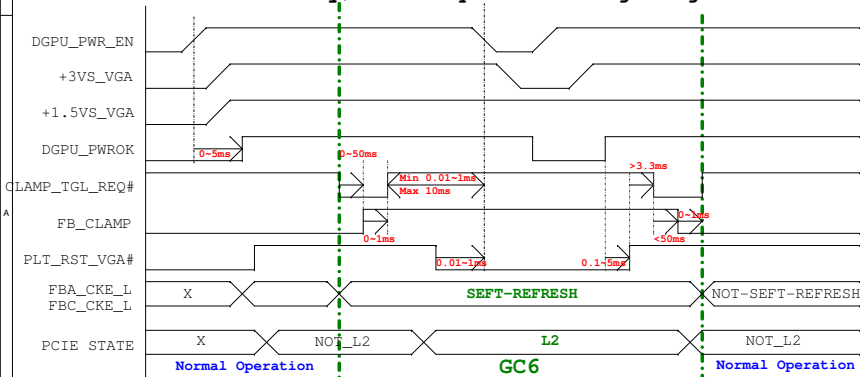
GPU Reset Sequence



Power sequencing violations



GC6 Entry/Exit Sequence Timing Diagram



For N14P-GV2 strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GV2	1 GHz	128M*16*4 1GB	Samsung K4W2G1646E-BC1A	R	R	R	R	R	R	R	R
N14P-GV2	1 GHz	128M*16*4 1GB	Micron MT41J128M16JT-093G-K	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K	PD 45K	PU 5K	PU 5K
N14P-GV2	1 GHz	128M*16*4 1GB	Hynix H5TQ2G63DFR-N0C	R	R	R	R	R	R	R	R
N14P-GV2	900 MHz	256M*16*4 2GB	Samsung K4W4G1646B-HC11	PU 45K	PD 45K	PD 15K	R	R	R	R	R
N14P-GV2	900 MHz	256M*16*4 2GB	Micron MT41K256M16HA-107G-E	R	R	R	R	R	R	R	R

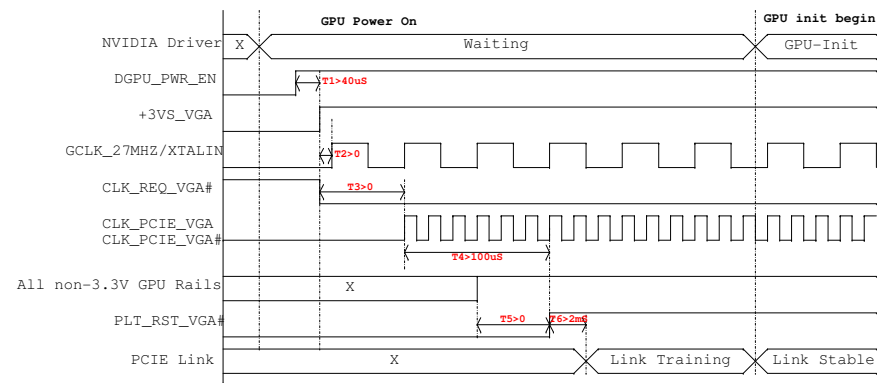
For N14P-GS strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GS	1 GHz	128M*16*8 2GB	Samsung K4W2G1646E-BC1A	R	R	R	R	R	R	R	R
N14P-GS	1 GHz	128M*16*8 2GB	Micron MT41J128M16JT-093G-K	PU 45K	PD 5K	PD 20K	PD 5K	PD 45K	PD 45K	PU 5K	PD 15K
N14P-GS	1 GHz	128M*16*8 2GB	Hynix H5TQ2G63DFR-N0C	R	R	R	R	R	R	R	R
N14P-GS	900 MHz	256M*16*8 2GB	Samsung K4W4G1646B-HC11	PU 45K	PD 5K	PD 20K	R	R	R	R	R
N14P-GS	900 MHz	256M*16*8 4GB	Micron MT41K256M16HA-107G-E	PU 45K	PD 5K	PD 20K	PD 5K	PD 45K	PD 10K	PU 5K	PD 15K

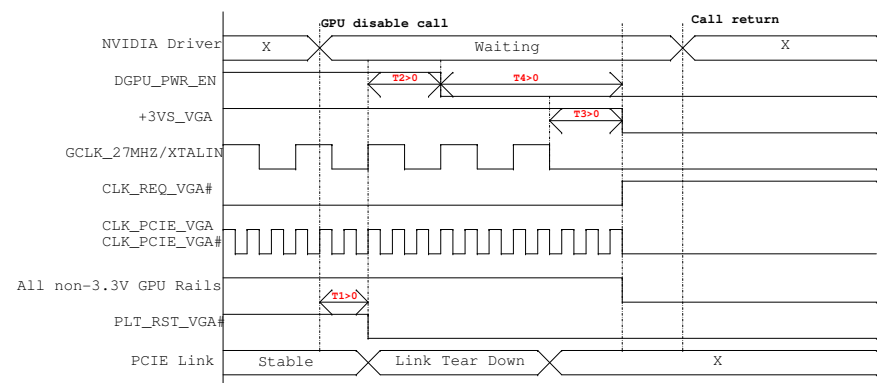
For N14M-GE strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14M-GE	1 GHz	128M*16*4 1GB	Samsung K4W2G1646E-BC1A	R	R	R	R	R	R	R	R
N14M-GE	1 GHz	128M*16*4 1GB	Micron MT41J128M16JT-093G-K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
N14M-GE	1 GHz	128M*16*4 1GB	Hynix H5TQ2G63DFR-N0C	R	R	R	R	R	R	R	R
N14M-GE	900 MHz	256M*16*4 2GB	Samsung K4W4G1646B-HC11	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
N14M-GE	900 MHz	256M*16*4 2GB	Micron MT41K256M16HA-107G-E	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K

Optimus Typical Power-Up Sequence



Optimus Typical Power-Down Sequence



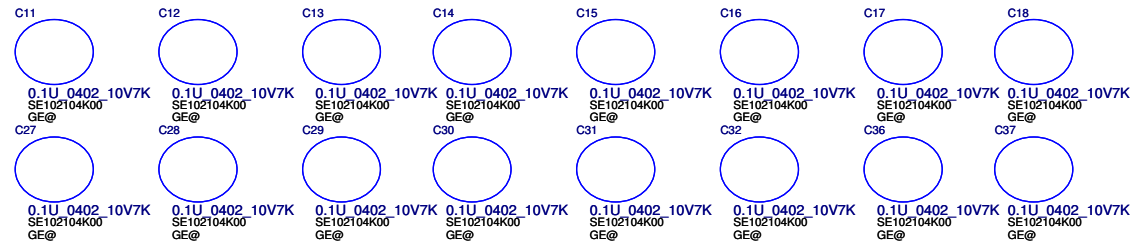
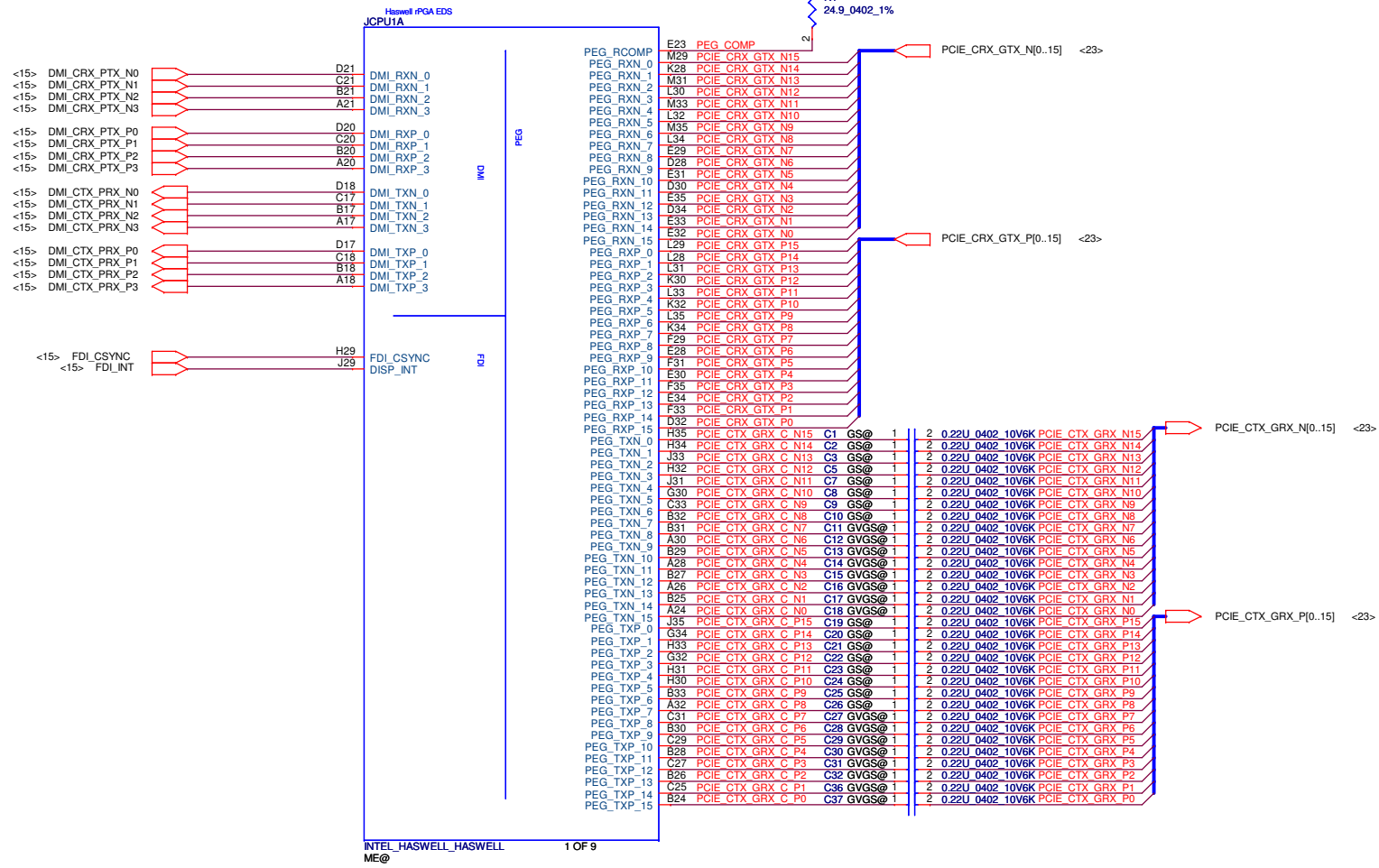
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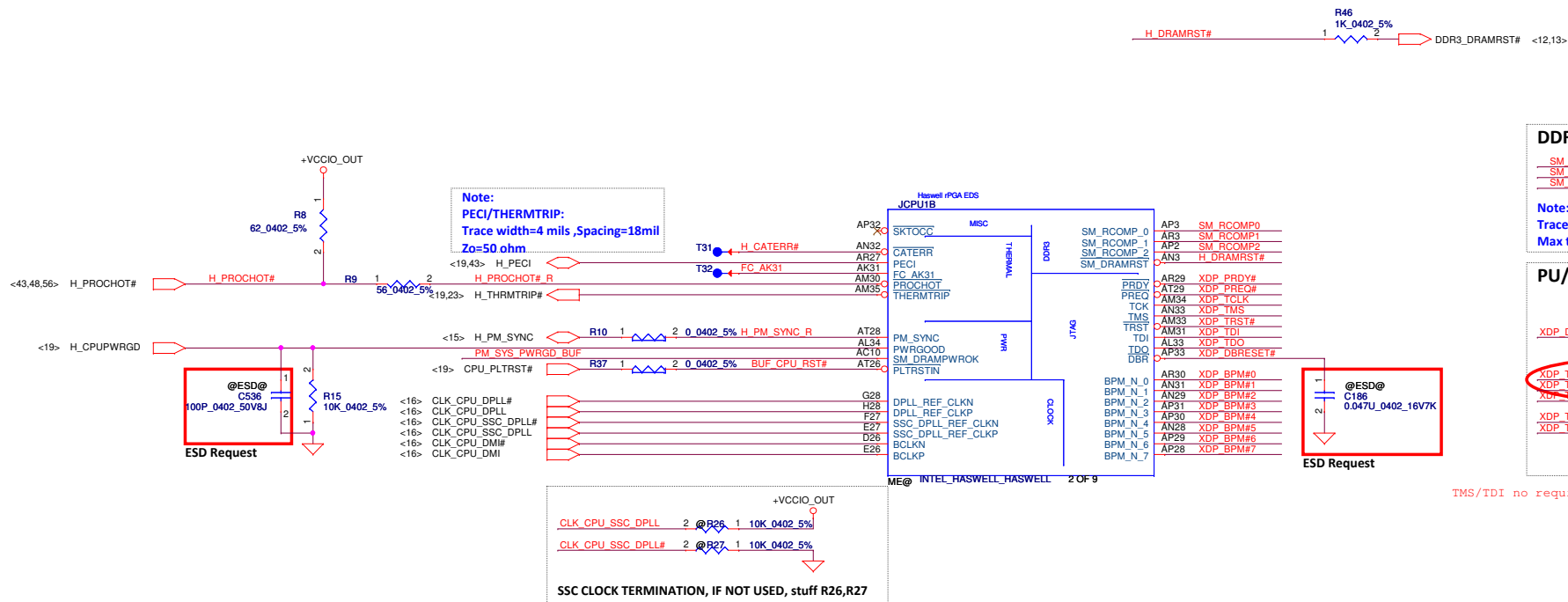
PCB
DA14@
DA6000Z1000
PCB 02N LA-A191P REV0 MB DIS 2



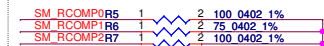
PCB
DA15@
DA6000Z1100
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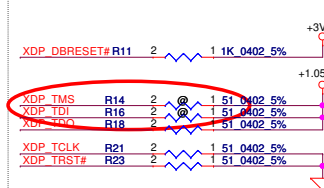


DDR3 COMPENSATION SIGNALS



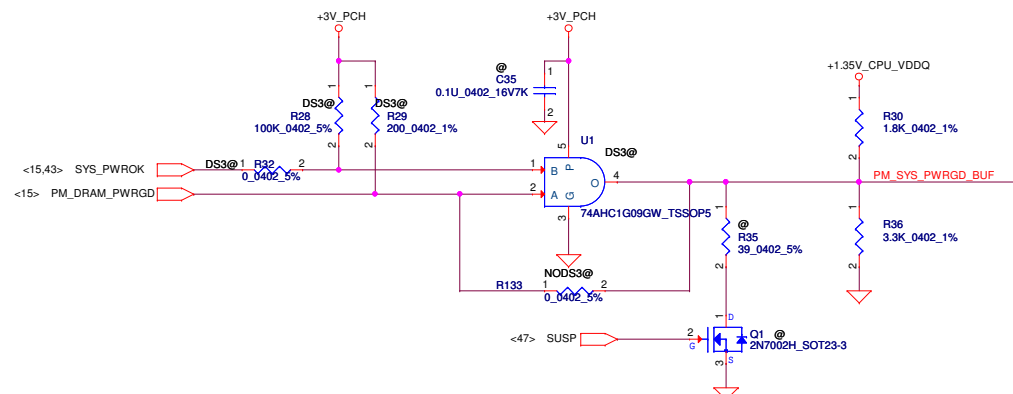
Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mils

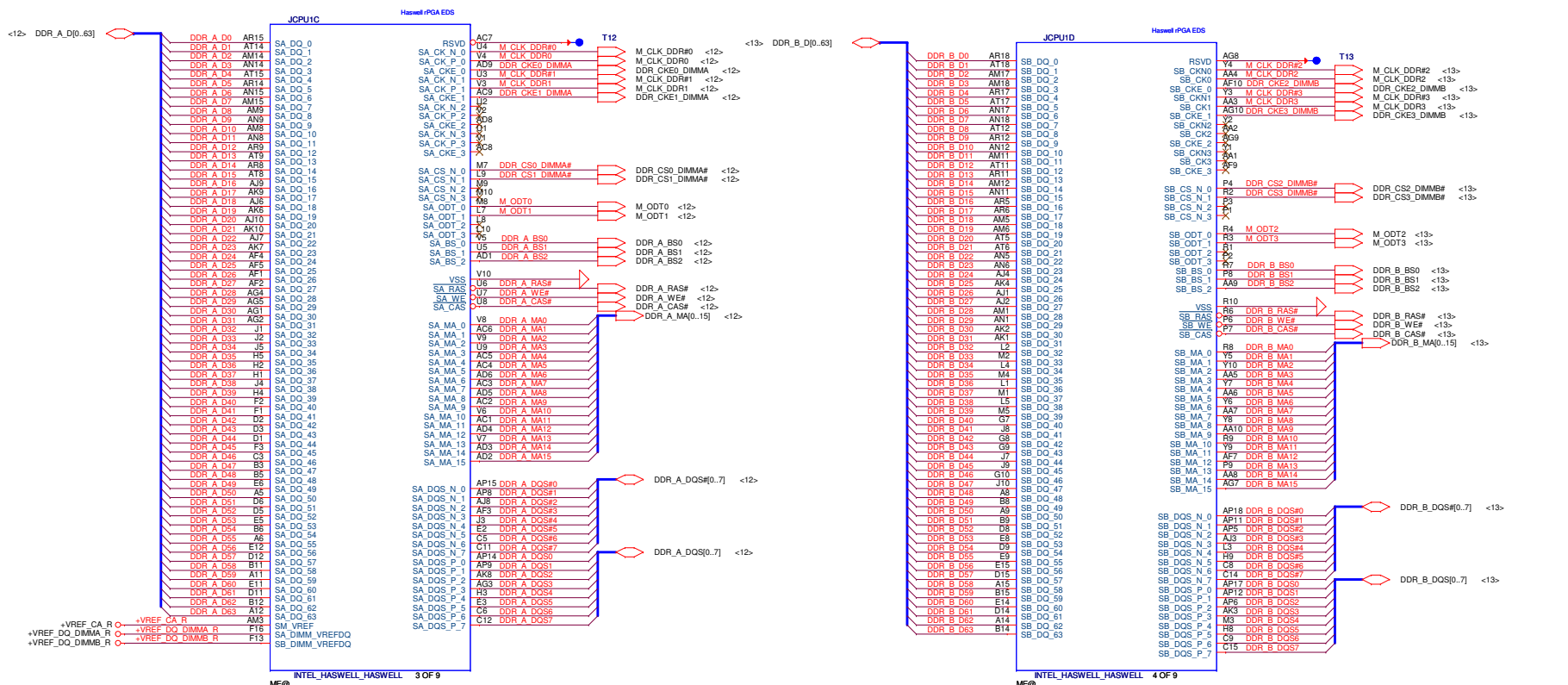
PU/PD for JTAG signals



TMS/TDI no require pull high on Check list

SM_DRAMPWROK with DDR Power Gating Topology





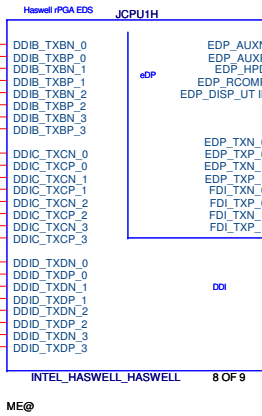
CPI DRIVER VREF PATH IS DEFAULT

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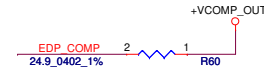
HDMI D2
HDMI D1
HDMI D0
HDMI CLK

HDMI

Place on connector side



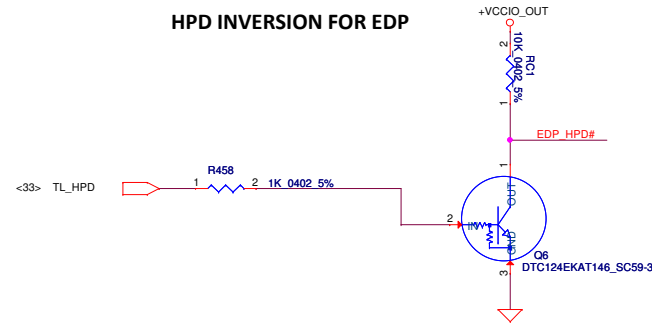
COMPENSATION PU FOR eDP



Note:

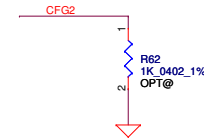
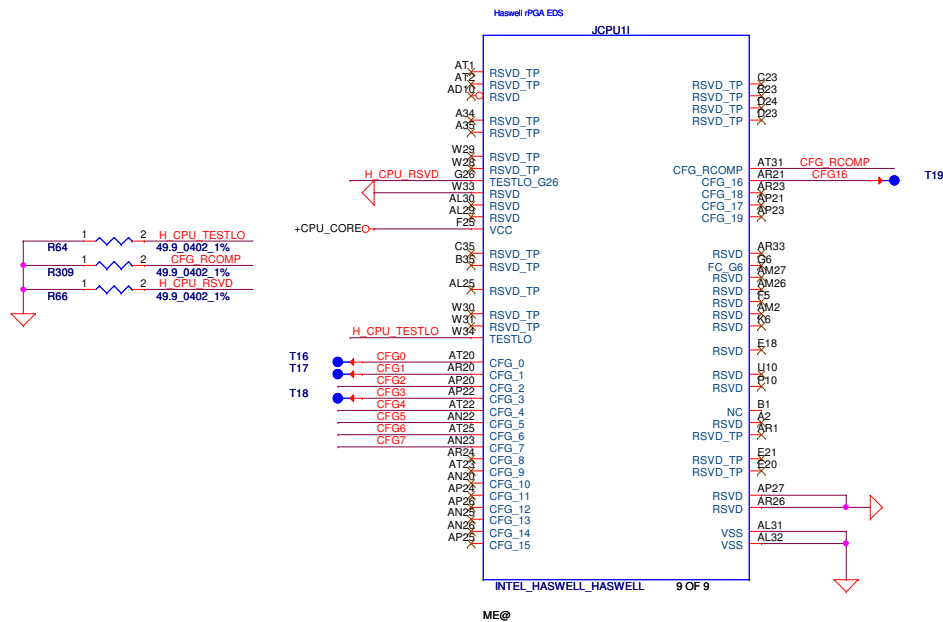
Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.

HPD INVERSION FOR EDP

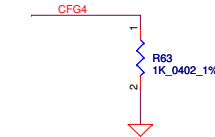


HPD is a active high signal from device. The HPD processor input is a low voltage active signal.

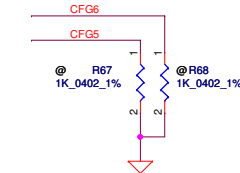
CFG Straps for Processor



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed



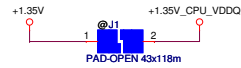
Embedded Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port ★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	★ 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

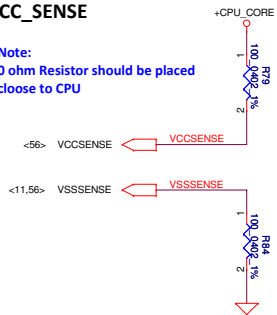
PEG DEFER TRAINING	
CFG7	★ 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

+1.35V_CPU_VDDQ Source

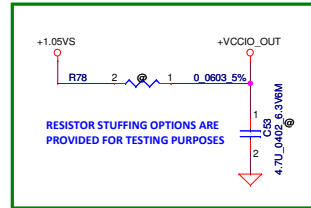
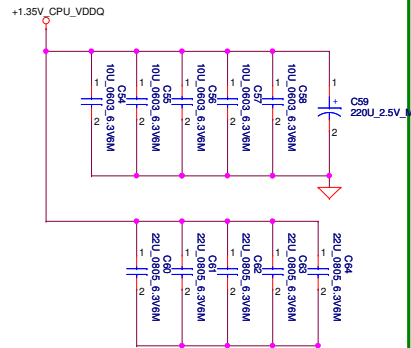


VCC_SENSE

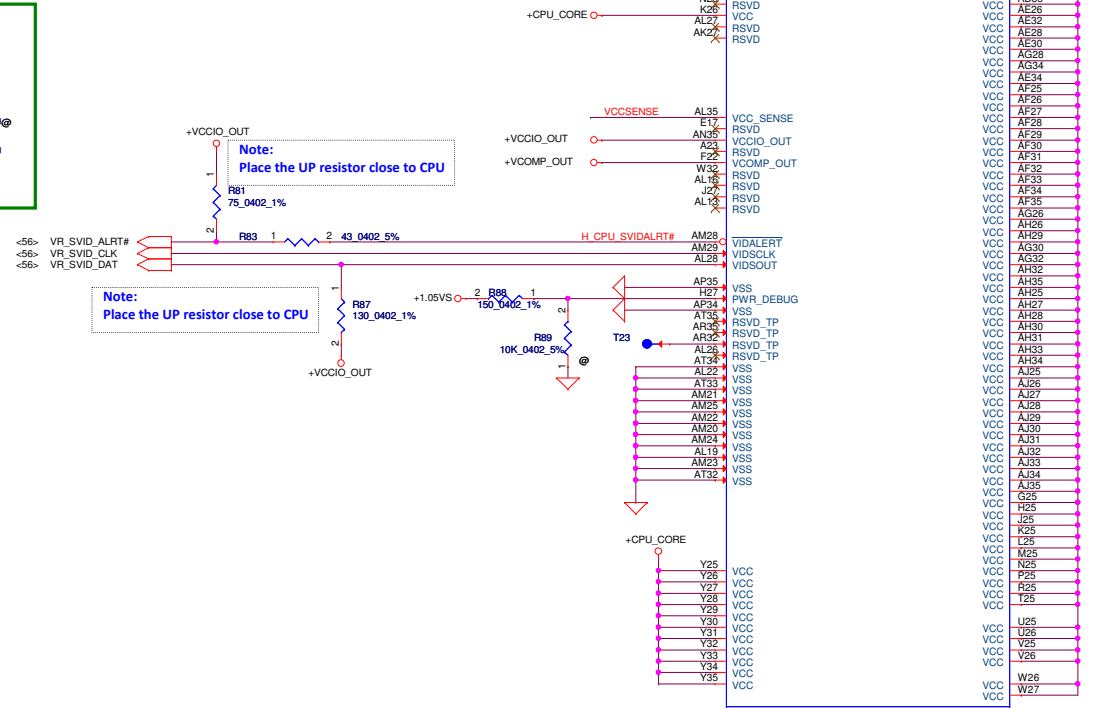
Note:
0 ohm Resistor should be placed
close to CPU



VDDQ DECOUPLING

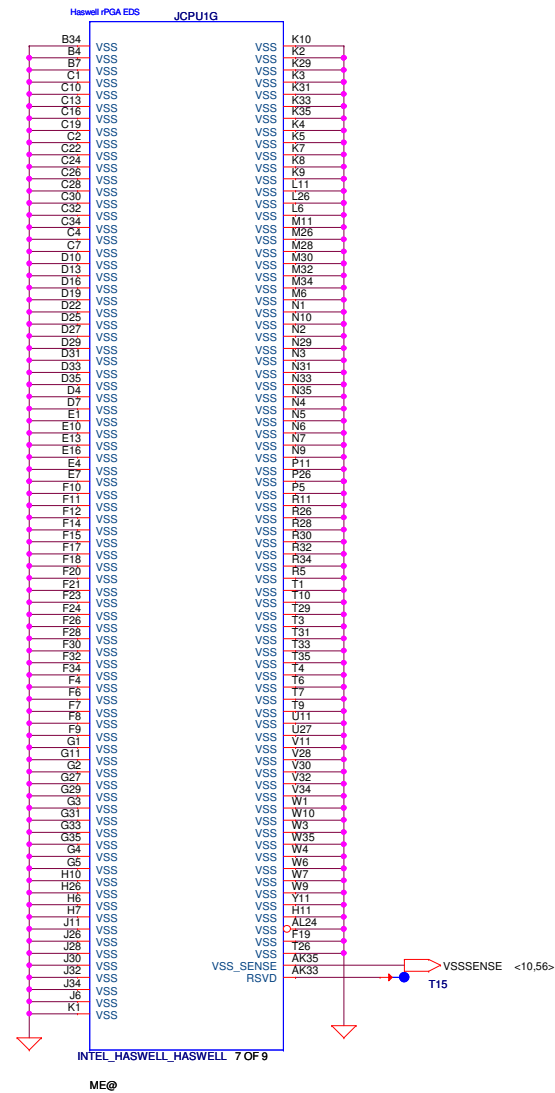
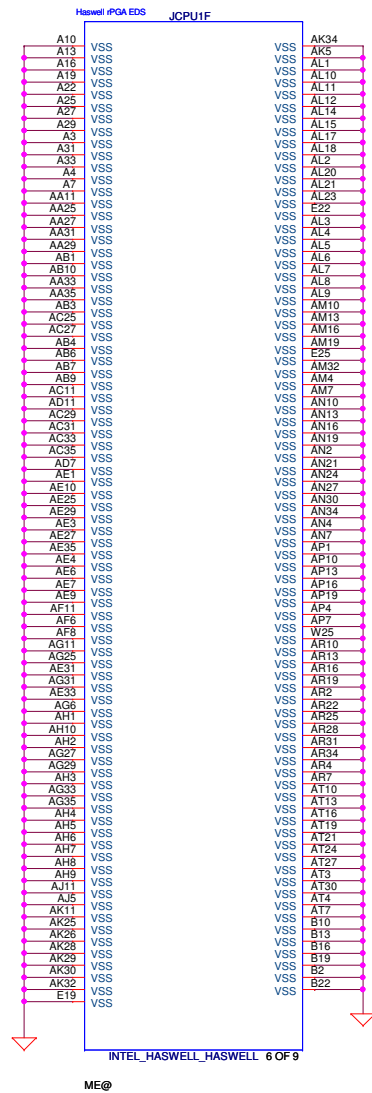


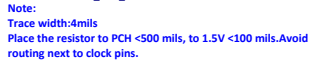
Note:
Place the UP resistor close to CPU



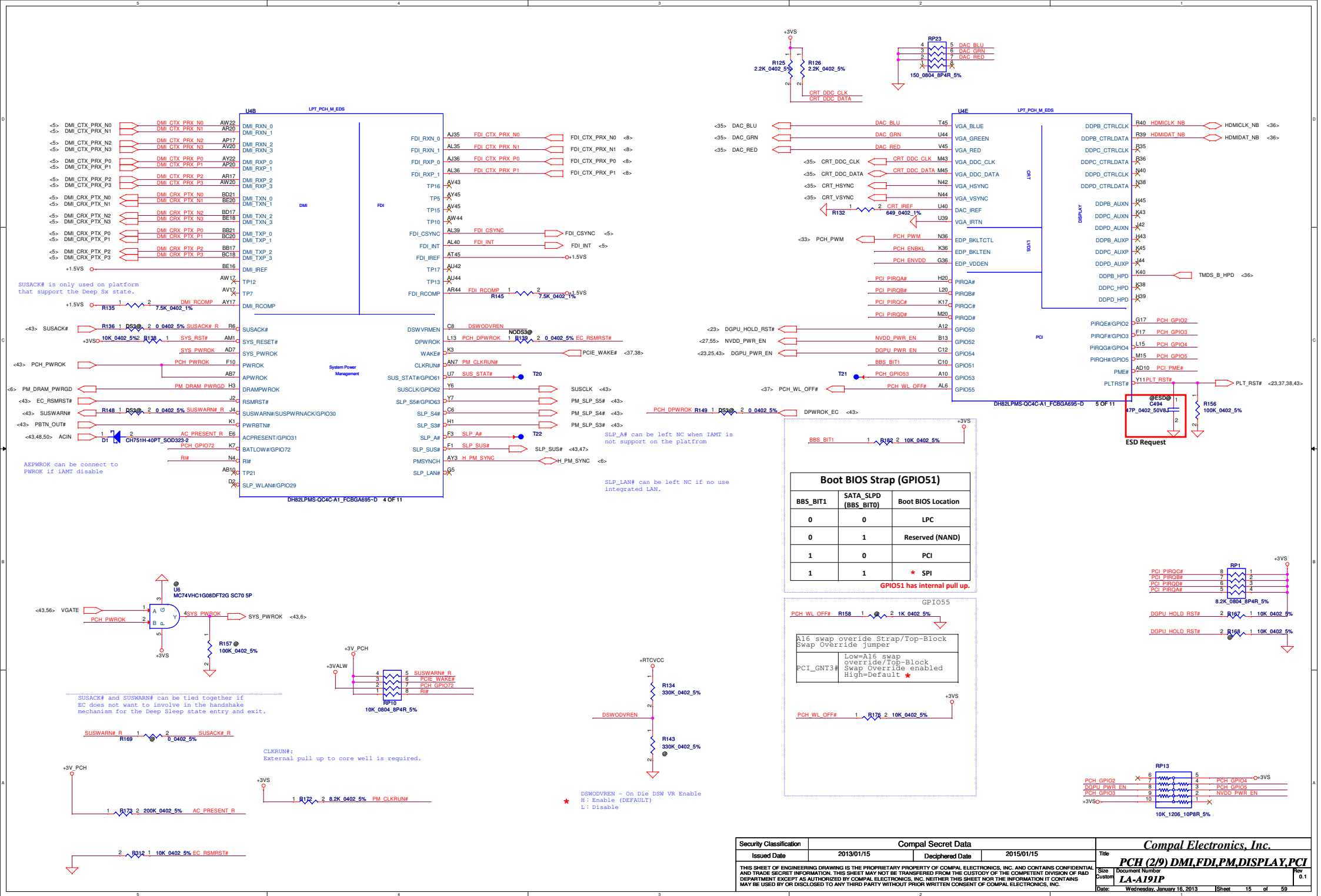
ME@

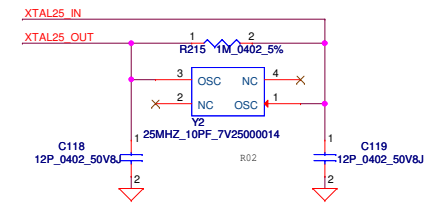
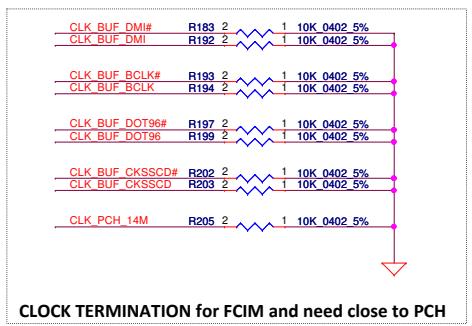
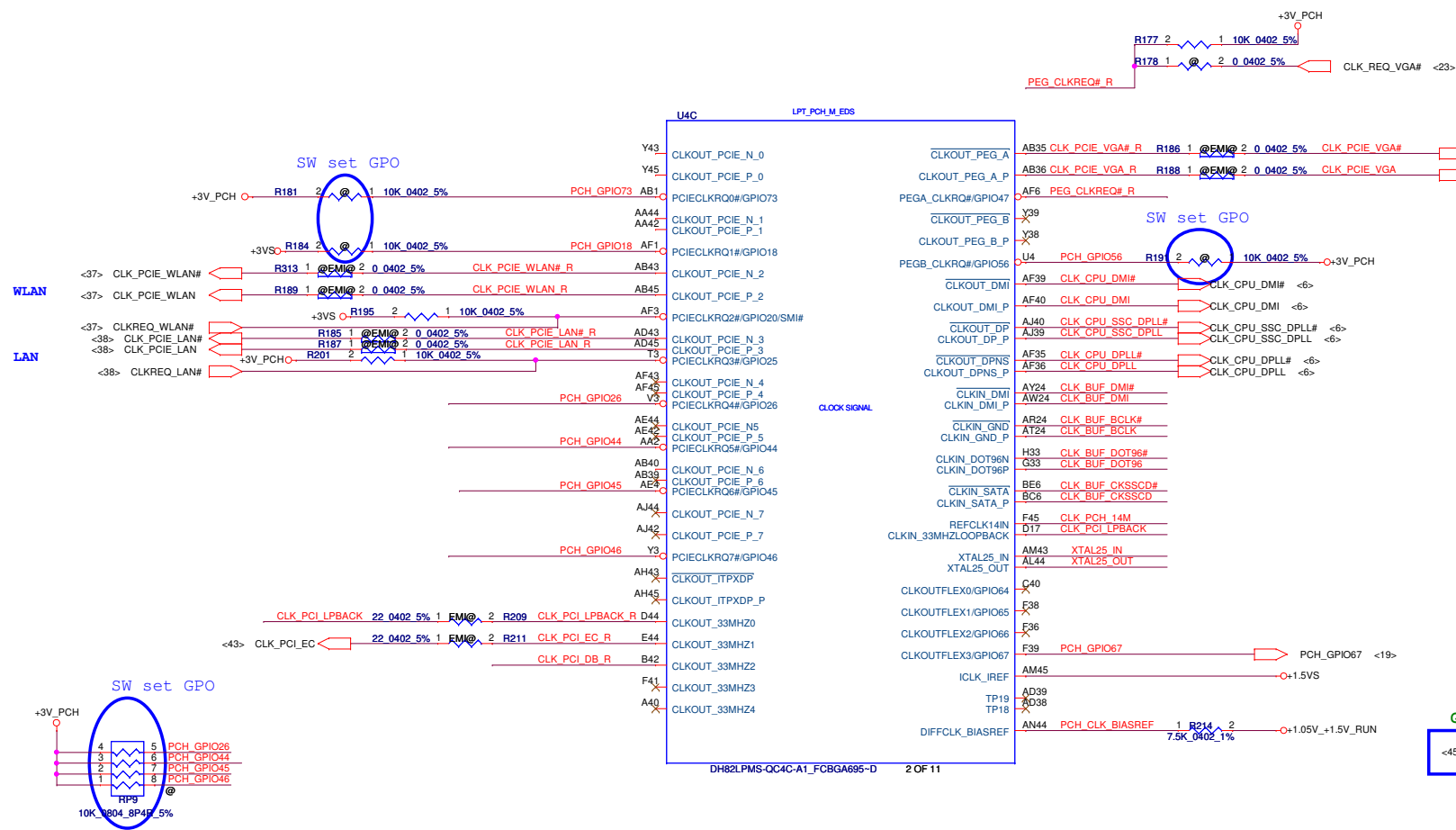
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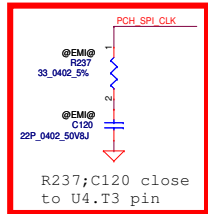


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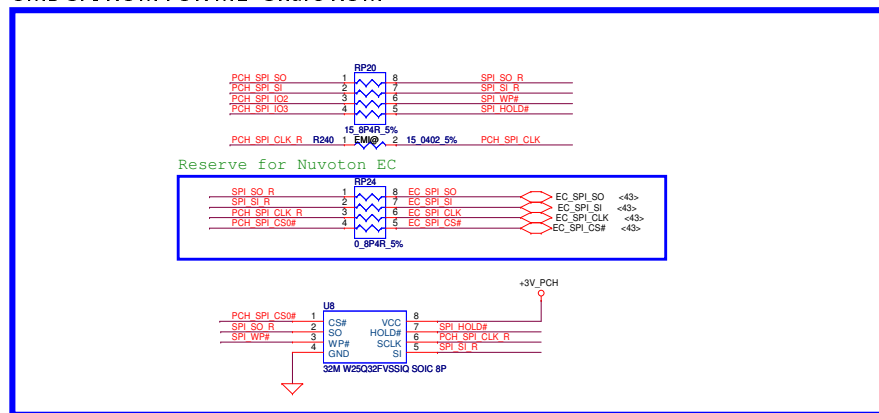


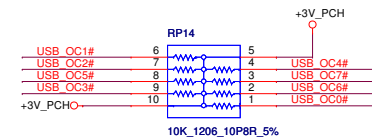


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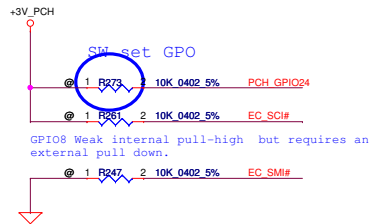


8MB SPI ROM FOR ME+Share ROM

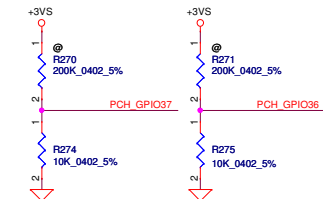
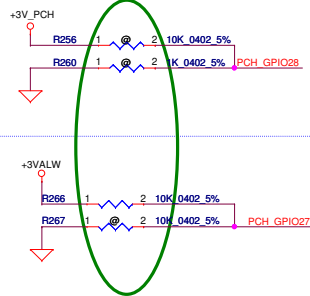




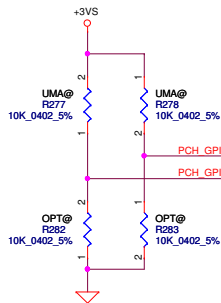
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Issued Date	2013/01/15	Deciphered Date	2015/01/15	Title	PCH (5/9) PCIE, USB	
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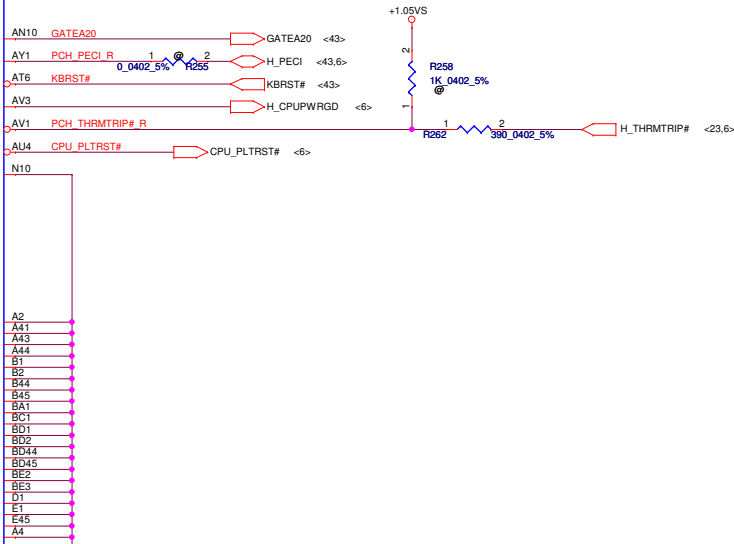
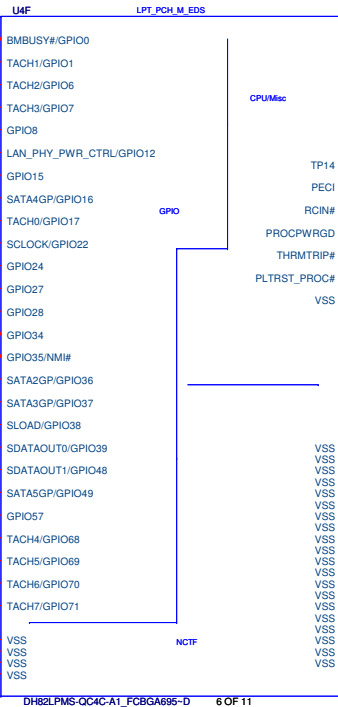
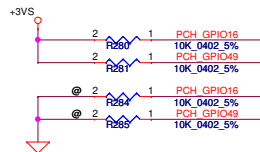
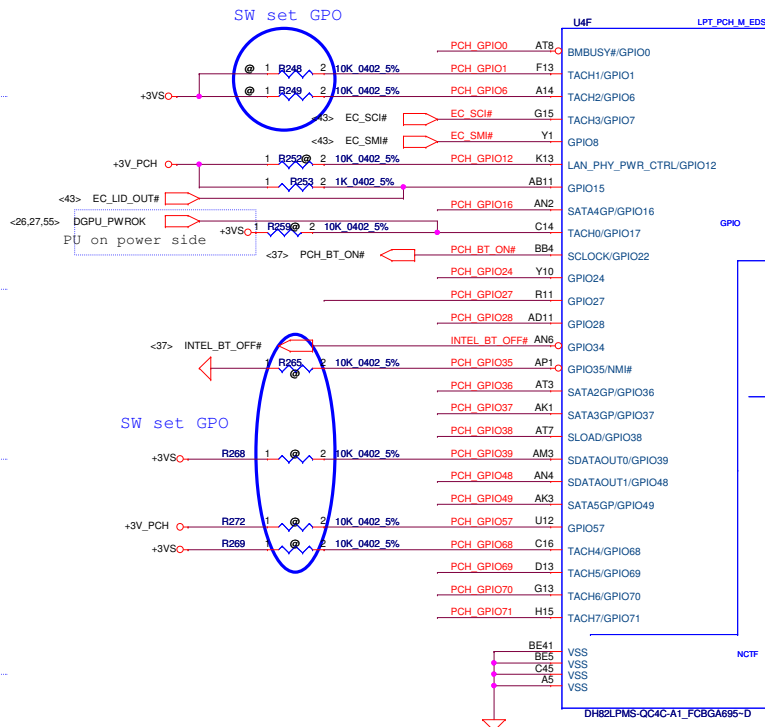
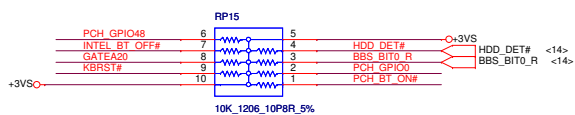
Remove strap description
inform SW set GPO



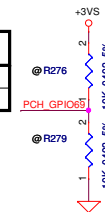
BIOS Request SKU ID



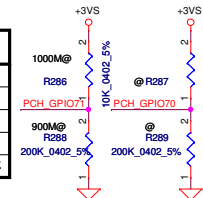
PCH_GPIO38	PCH_GPIO67	Function
0	0	MUXLESS
0	1	Reserved
1	0	DIS
1	1	UMA

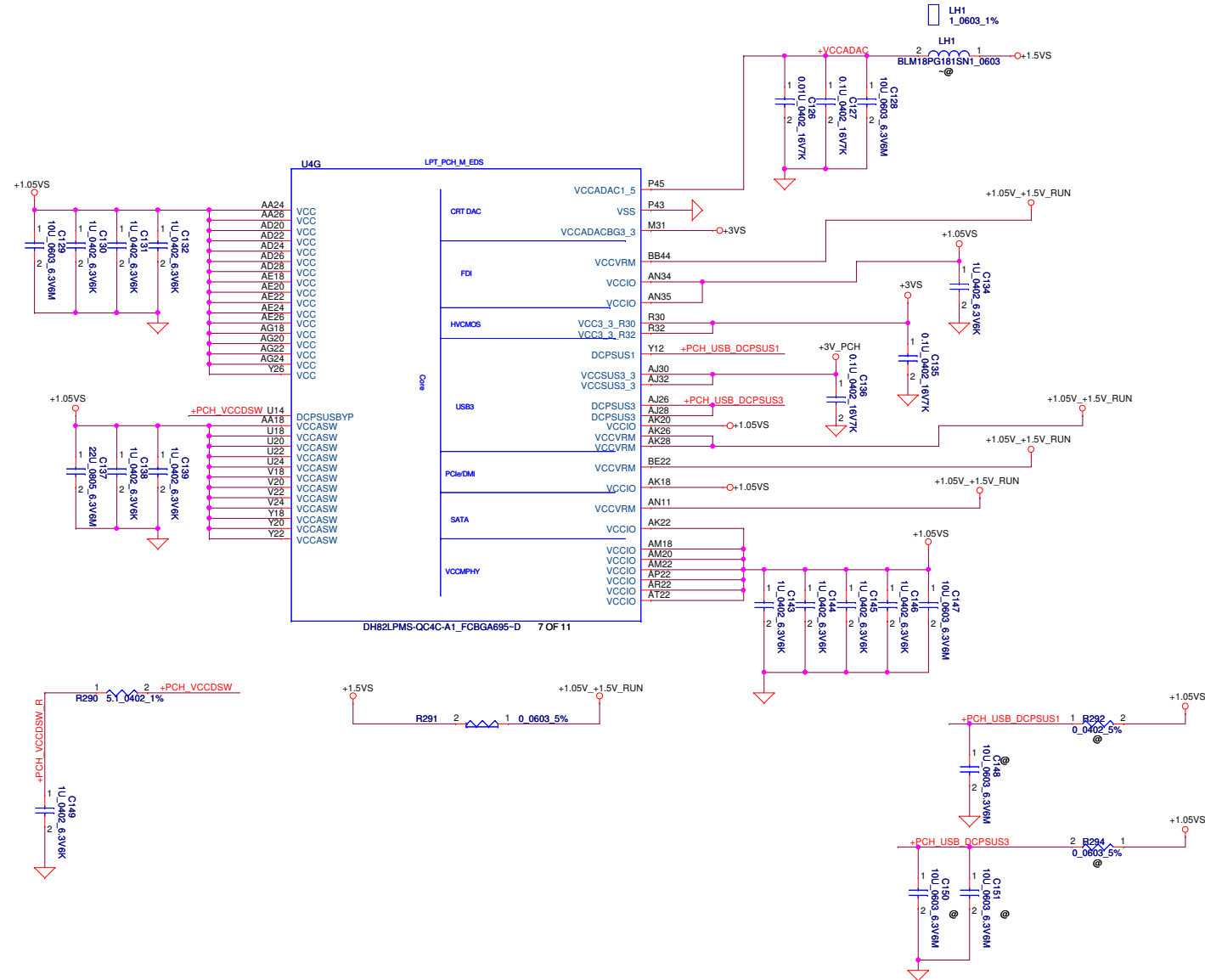


PCH_GPIO69	Function
0	
1	

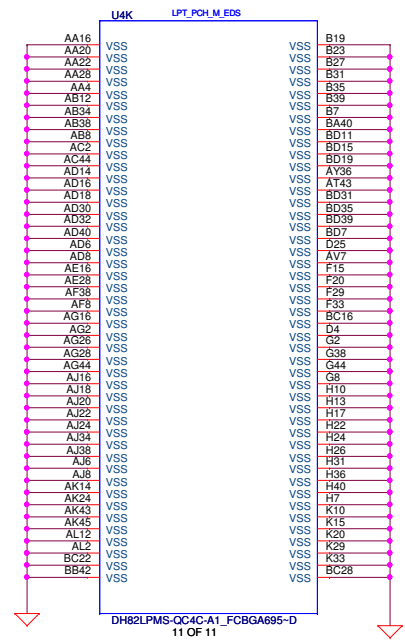
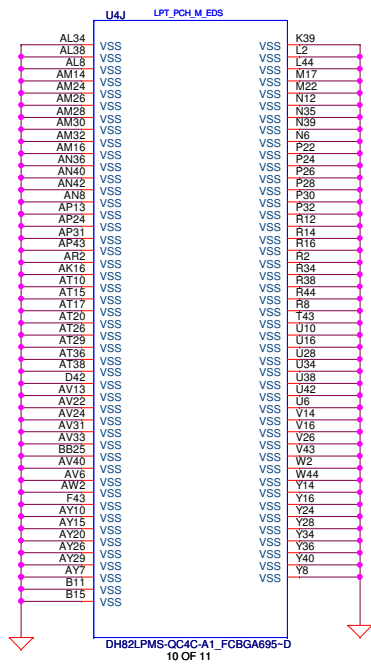


PCH_GPIO70	Function
0	
1	





PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADM_1_5	1.5V	0.070 A
VCCADM_3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A



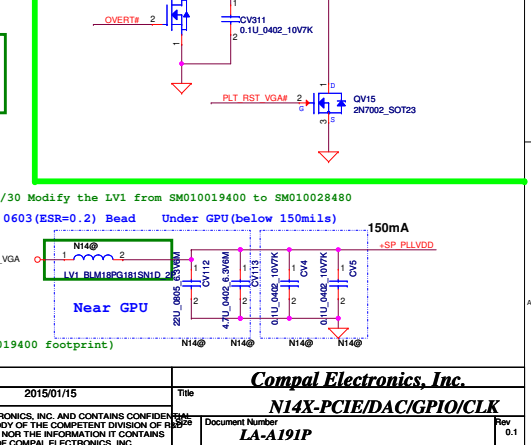
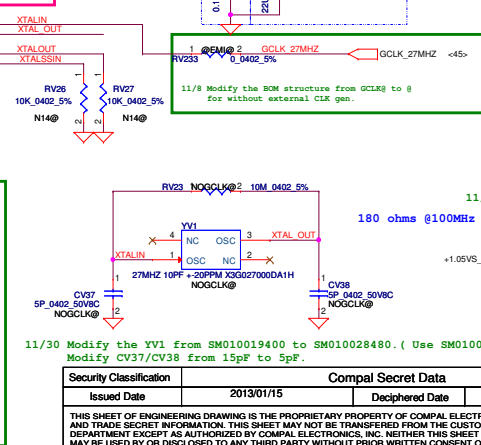
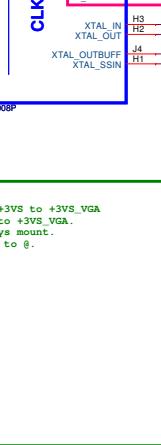
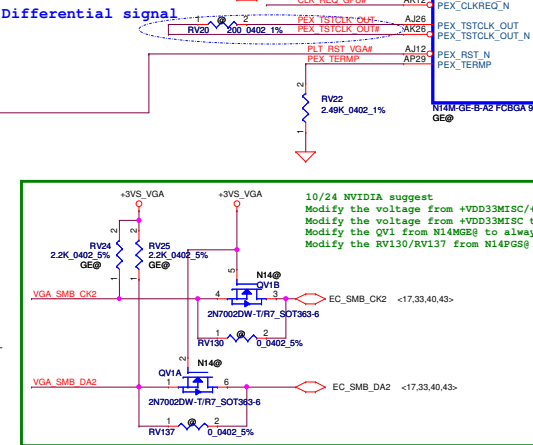
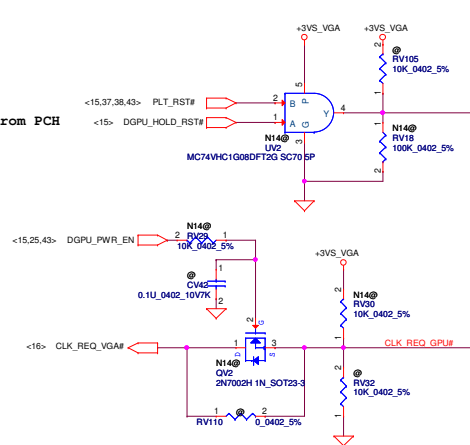
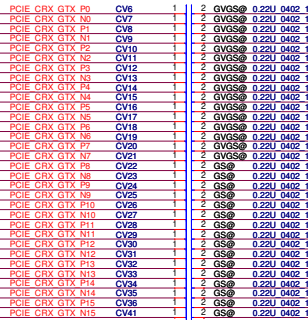
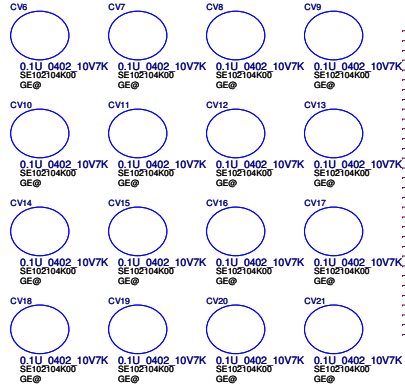
<5> PCIE_CTX_GRP_N0..15] <5> PCIE_CTX_GRP_P0..15] <5> PCIE_CTX_GRP_N0..15] <5> PCIE_CTX_GRP_P0..15]

U65 N14P-GV2-B-A2 BGA 908P SA000065500 GV2@

U65 N14P-GS-A2 BGA 908P SA000065F00 GS@

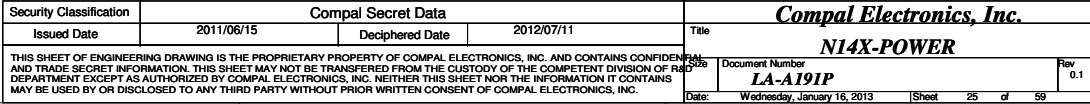
Non-support PCIE port8-15:N14M-GM and N14P-GV2

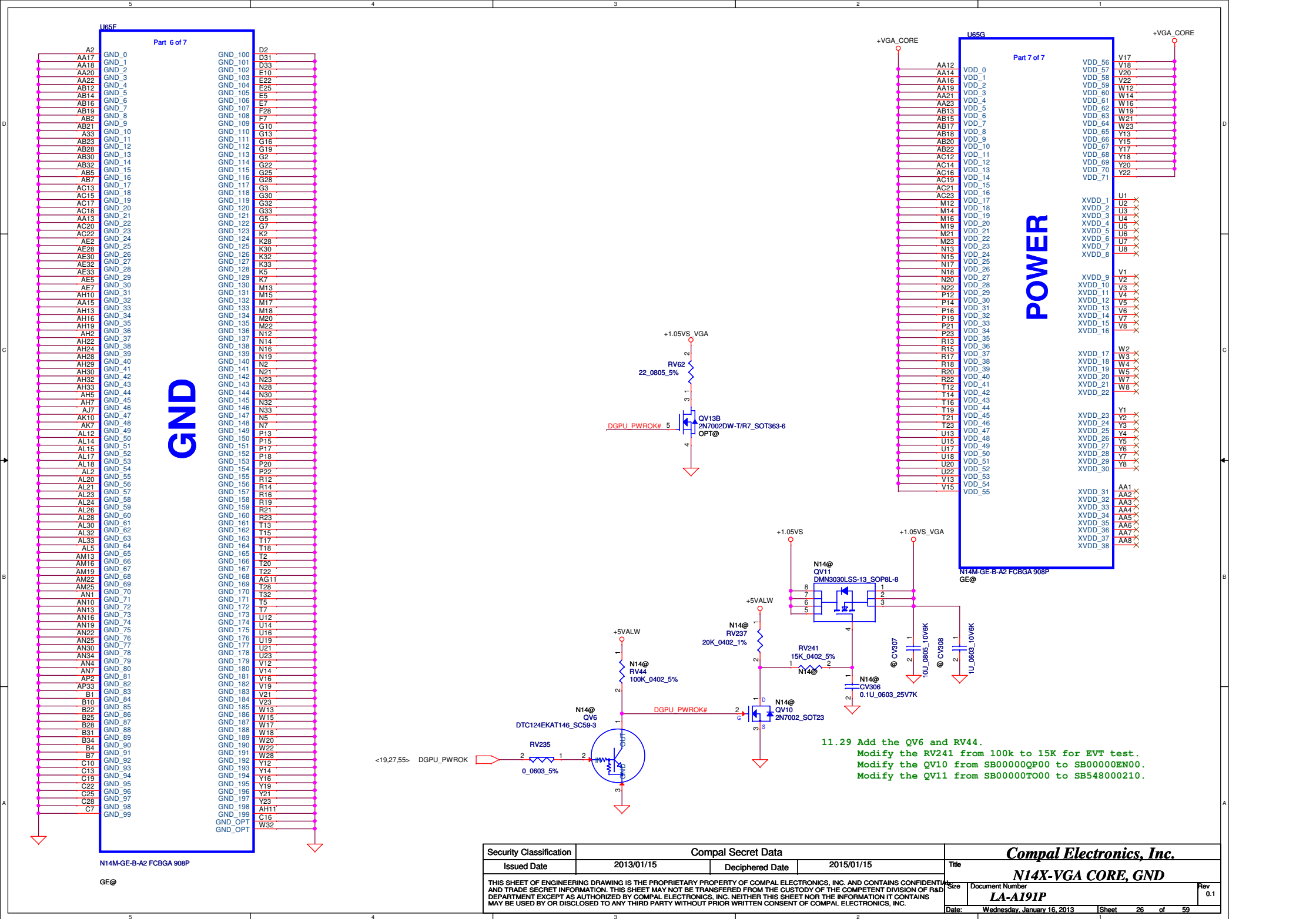
Support PCIE port8-15:N14P-GS

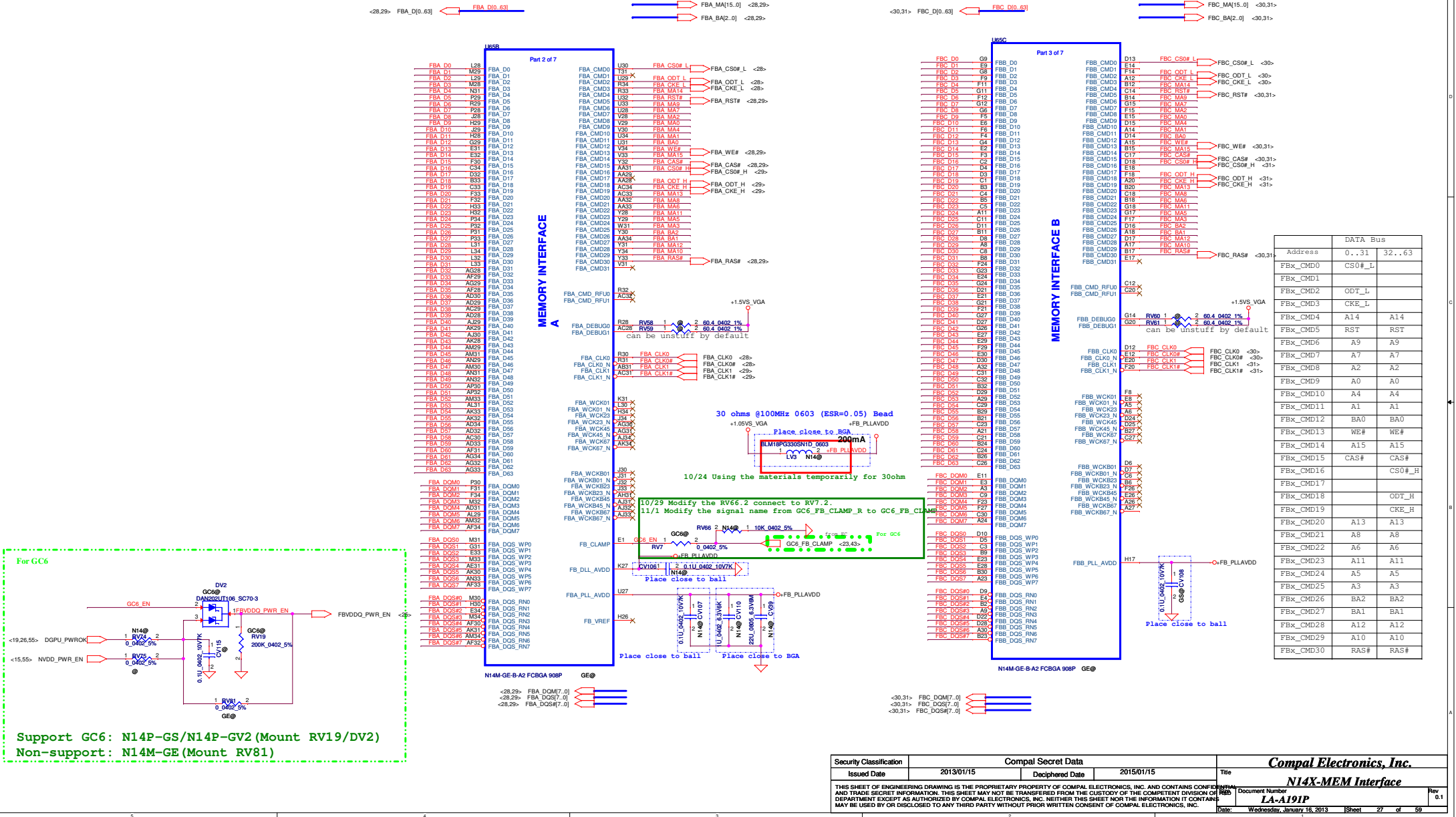


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N14X-PCIE/DAC/GPIO/CLK	
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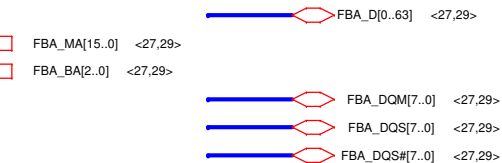
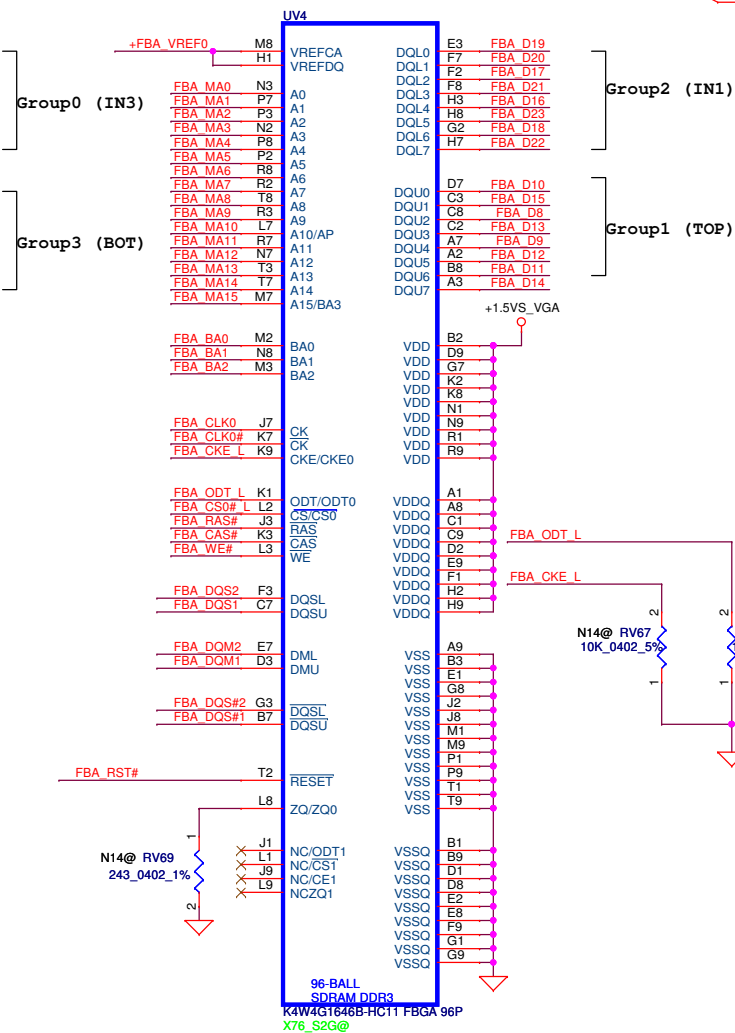
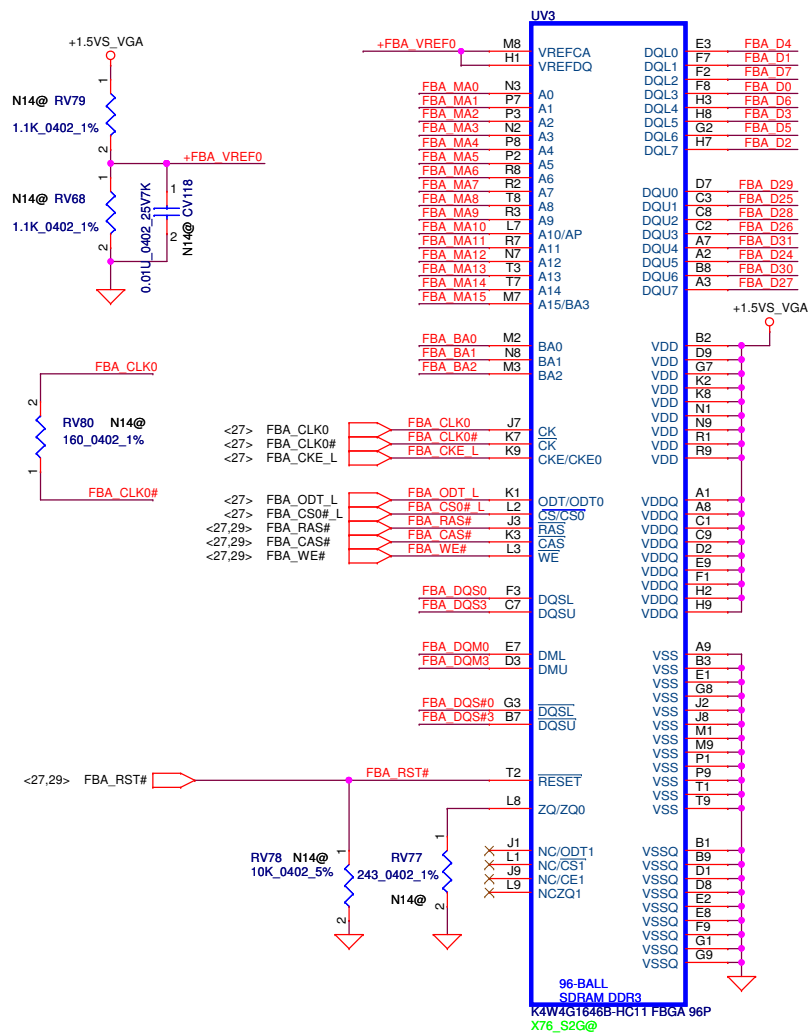




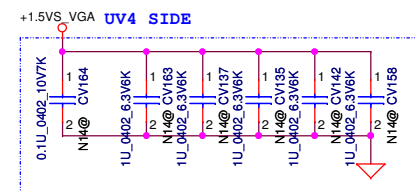
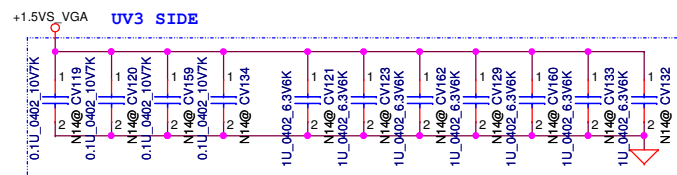
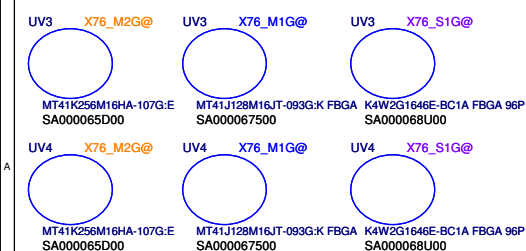


Support GC6: N14P-GS/N14P-GV2 (Mount RV19/DV2)
Non-support: N14M-GE (Mount RV81)

Memory Partition A - Lower 32 bits

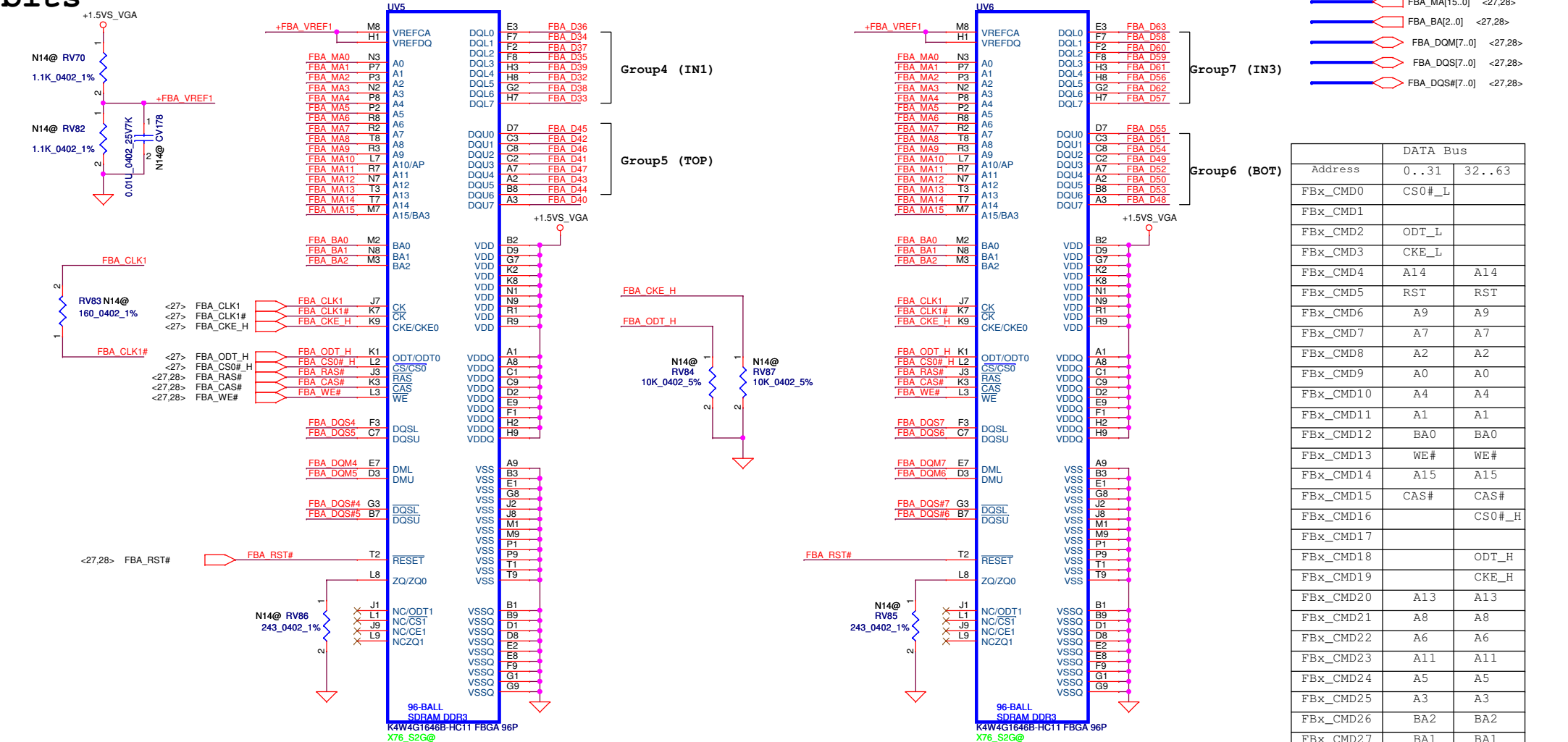


	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

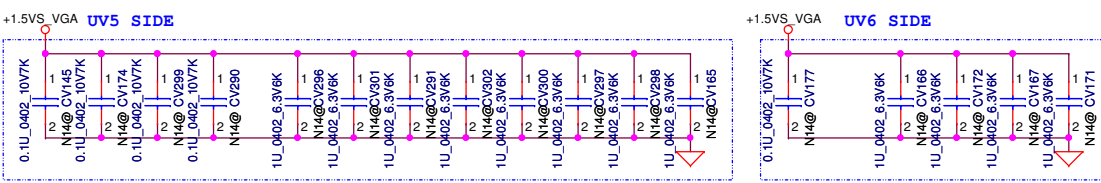
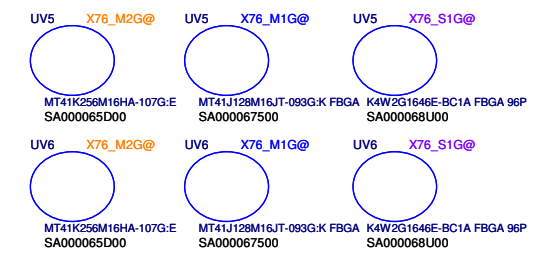


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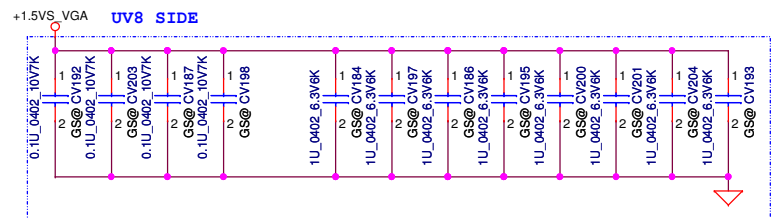
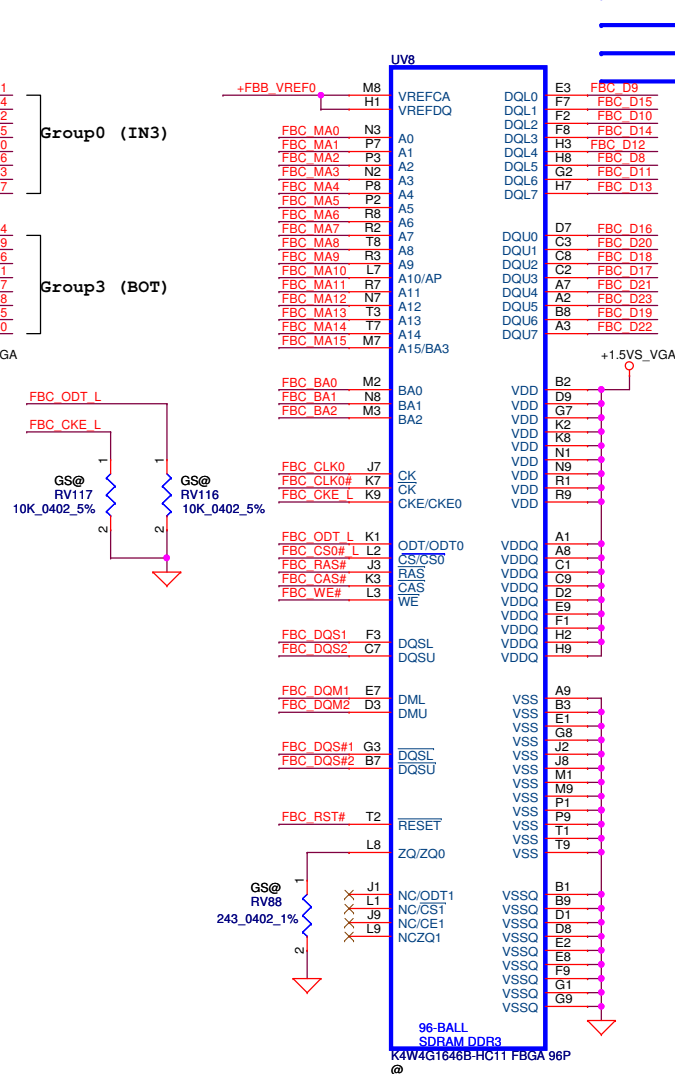
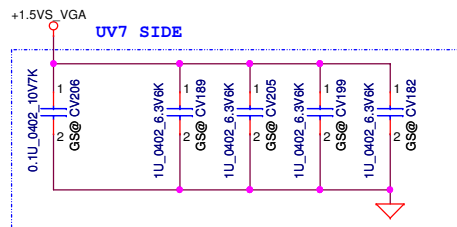
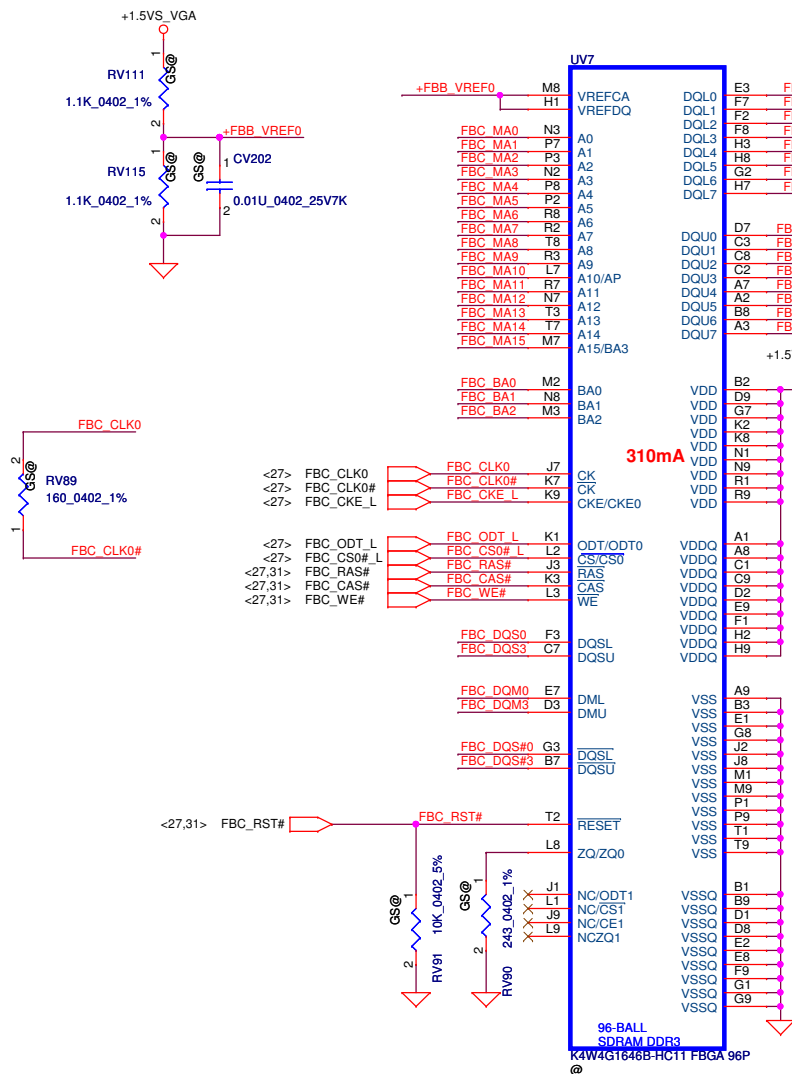
Memory Partition A - Upper 32 bits



DATA Bus		
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



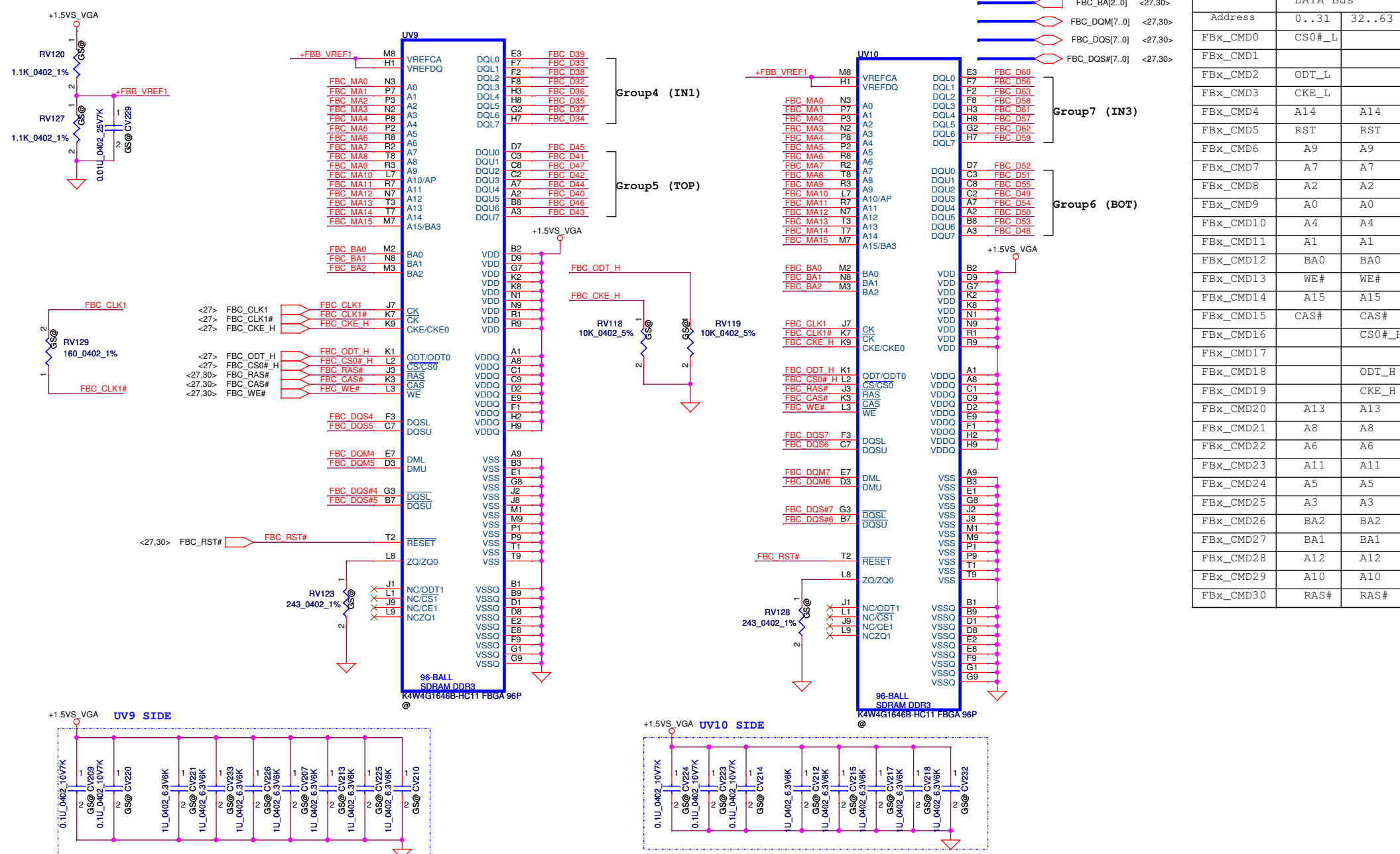
Memory Partition C - Lower 32 bits



	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

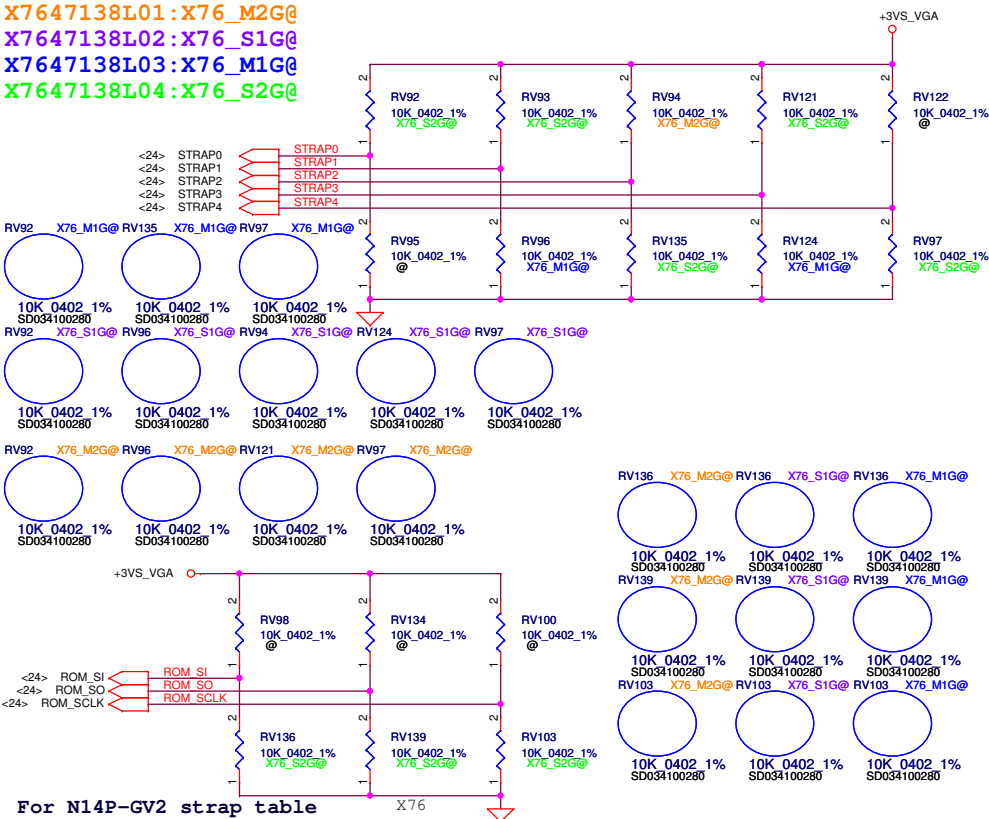
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Memory Partition C - Upper 32 bits



DATA Bus		
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16	CS0#_H	
FBx_CMD17		
FBx_CMD18	ODT_H	
FBx_CMD19	CKE_H	
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

X7647138L01:X76_M2G@
X7647138L02:X76_S1G@
X7647138L03:X76_M1G@
X7647138L04:X76_S2G@



For N14P-GV2 strap table

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GV2	1 GHz	128M* 16" 4	Samsung K4W2G1646E-BC1A	R	R	R	R	R	R	R	R
N14P-GV2	1 GHz	128M* 16" 4	Micron MT41J128M16JT-093G.K	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K	PD 45K	PU 5K	PU 5K
N14P-GV2	1 GHz	128M* 16" 4	Hynix H5TQ2G63DFR-N0C	PU 45K	R	R	R	R	PD 30K	PU 5K	PU 5K
N14P-GV2	900 MHz	256M* 16" 4	Samsung K4W4G1646B-HC11	R	R	R	R	R	R	R	R
N14P-GV2	900 MHz	256M* 16" 4	Micron MT41K256M16HA-107G.E	PU 45K	PD 45K	PD 15K	PD 5K	PD 45K	PD 20K	PU 5K	PU 5K

For N14P-GS strap table

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GS	1 GHz	128M* 16" 8	Samsung K4W2G1646E-BC1A	R	R	R	R	R	R	R	R
N14P-GS	1 GHz	128M* 16" 8	Micron MT41J128M16JT-093G.K	PU 45K	PD 5K	PD 20K	PD 5K	PD 45K	PD 45K	PU 5K	PD 15K
N14P-GS	1 GHz	128M* 16" 8	Hynix H5TQ2G63DFR-N0C	PU 45K	PD 5K	PD 20K	PD 5K	PD 45K	PD 35K	PU 5K	PD 15K
N14P-GS	900 MHz	256M* 16" 8	Samsung K4W4G1646B-HC11	PU 45K	PD 5K	PD 20K	PD 5K	PD 45K	PD 20K	PU 5K	PD 15K
N14P-GS	900 MHz	256M* 16" 8	Micron MT41K256M16HA-107G.E	PU 45K	PD 5K	PD 20K	PD 5K	PD 45K	PD 10K	PU 5K	PD 15K

For N14M-GE strap table

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14M-GE	1 GHz	128M* 16" 4	Samsung K4W2G1646E-BC1A	R	R	R	R	R	R	R	R
N14M-GE	1 GHz	128M* 16" 4	Micron MT41J128M16JT-093G.K	PU 10K	PD 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
N14M-GE	1 GHz	128M* 16" 4	Hynix H5TQ2G63DFR-N0C	PU 10K	PD 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K
N14M-GE	900 MHz	256M* 16" 4	Samsung K4W4G1646B-HC11	R	R	R	R	R	R	R	R
N14M-GE	900 MHz	256M* 16" 4	Micron MT41K256M16HA-107G.E	PU 10K	PD 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K	PD 10K

VRAM Part Number

Freq.	Memory Size	Samsung K4W2G1646E-BC1A	Micron MT41J128M16JT-093G.K	Hynix H5TQ2G63DFR-N0C	Samsung K4W4G1646B-HC11	Micron MT41K256M16HA-107G.E
1 GHz	128M* 16" 8	SA000068U00	SA000067500	SA000065300		
900 MHz	256M* 16" 8				SA000068R00	SA000065D00

Multi-Level Mode

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Binary-Level Mode

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Physical Strapping pin	Strapping Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10K	PD
ROM_SI	SUB_VENDOR	10K	PU (VBIOS ROM) PD (Non-VBIOS ROM)
ROM_SO	VGA_DEVICE	10K	PD (No display)
STRAP0	RAM_CFG[0]	10K	PU (Binary=1) PD (Binary=0)
STRAP1	RAM_CFG[1]	10K	
STRAP2	RAM_CFG[2]	10K	
STRAP3	RAM_CFG[3]	10K	
STRAP4	PCIE_MAX_SPEED	10K	PD

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	Non-Primary 3D Acceleration Device (Class Code 302h)
1	Primary Display or VGA Device (Class Code 300h)

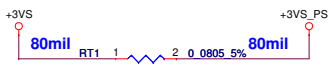
USER Straps	
User [3:0]	
1000-1100	Customer defined

PCI_DEVID						
GPU Type	DEVID[5]	DEVID[4]	DEVID[3]	DEVID[2]	DEVID[1]	DEVID[0]
N14P-GV2	0	1	0	0	1	0
N14P-GS	1	0	0	0	1	1

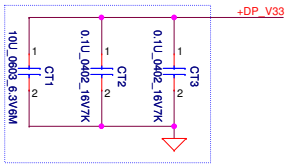
3GIO_PADCFG	
[3:0]	Description
0110	Gen 1 / Gen 2 Support only
0000	Gen 3 Support

PCIE_SPEED_CHANGE_GEN3		PCIE_MAX_SPEED	
N14P-GV2	1	1	
N14P-GS	1	1	
0: Disable PCIE Gen3 operation 1: Enable PCIE Gen3 operation		0: Limit to PCIE Gen1 1: PCIE Gen 2/3 Capable	
3GIO_PADCFG[3:0]			
Strap1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]
N14P-GV2	0	1	1
N14P-GS	0	0	0

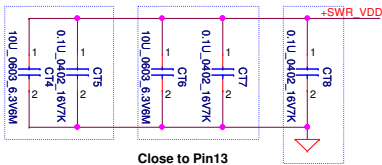
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Close to Pin3

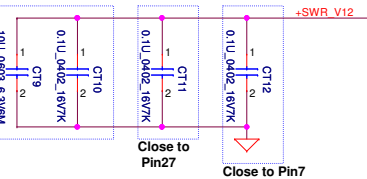


Close to LT2



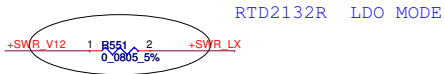
Close to Pin13

Close to Pin11



Close to Pin27

Close to Pin7



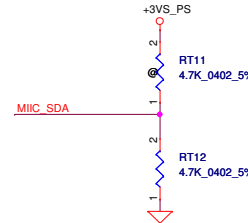
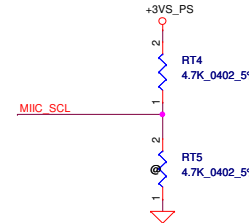
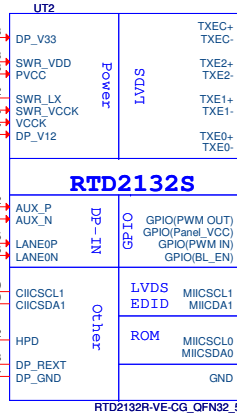
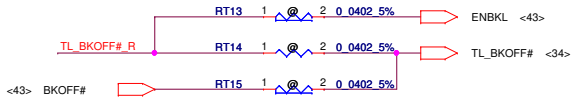
+3VS_PS

<8> EDP_CPU_AUX
<8> EDP_CPU_AUX#
<8> EDP_CPU_LANE_P0
<8> EDP_CPU_LANE_N0

C190 1 2 0.1U 0402 16V7K
C191 1 2 0.1U 0402 16V7K
C192 1 2 0.1U 0402 16V7K
C193 1 2 0.1U 0402 16V7K

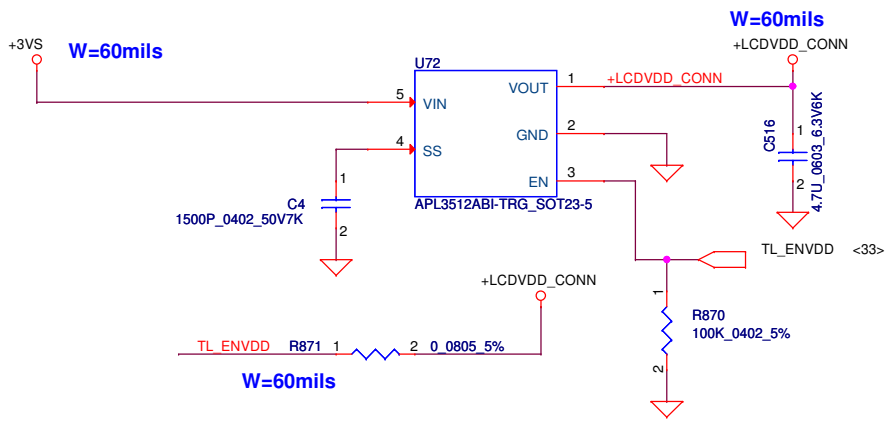


Vendor advise reserve it

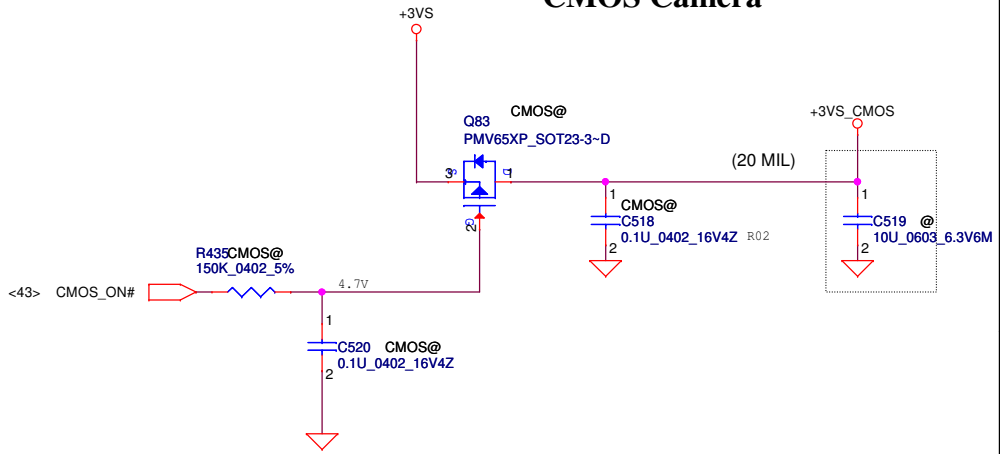


MIIC_SCL \ MIIC_SDA	MIIC_SDA	
	0	1
0	X	EC CODE
1	Internal ROM	EEPROM

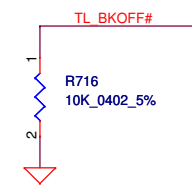
LCD POWER CIRCUIT



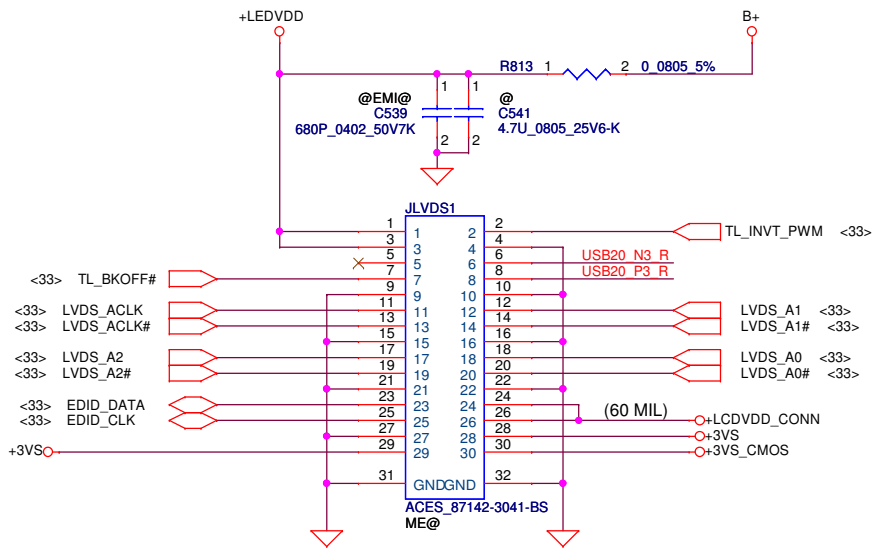
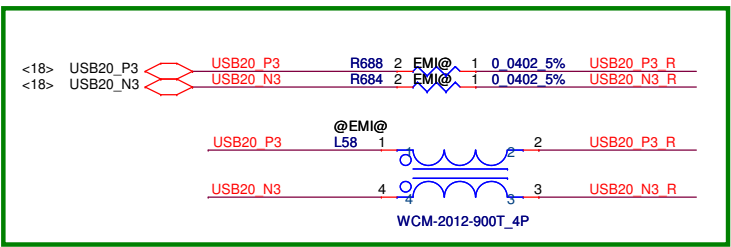
CMOS Camera



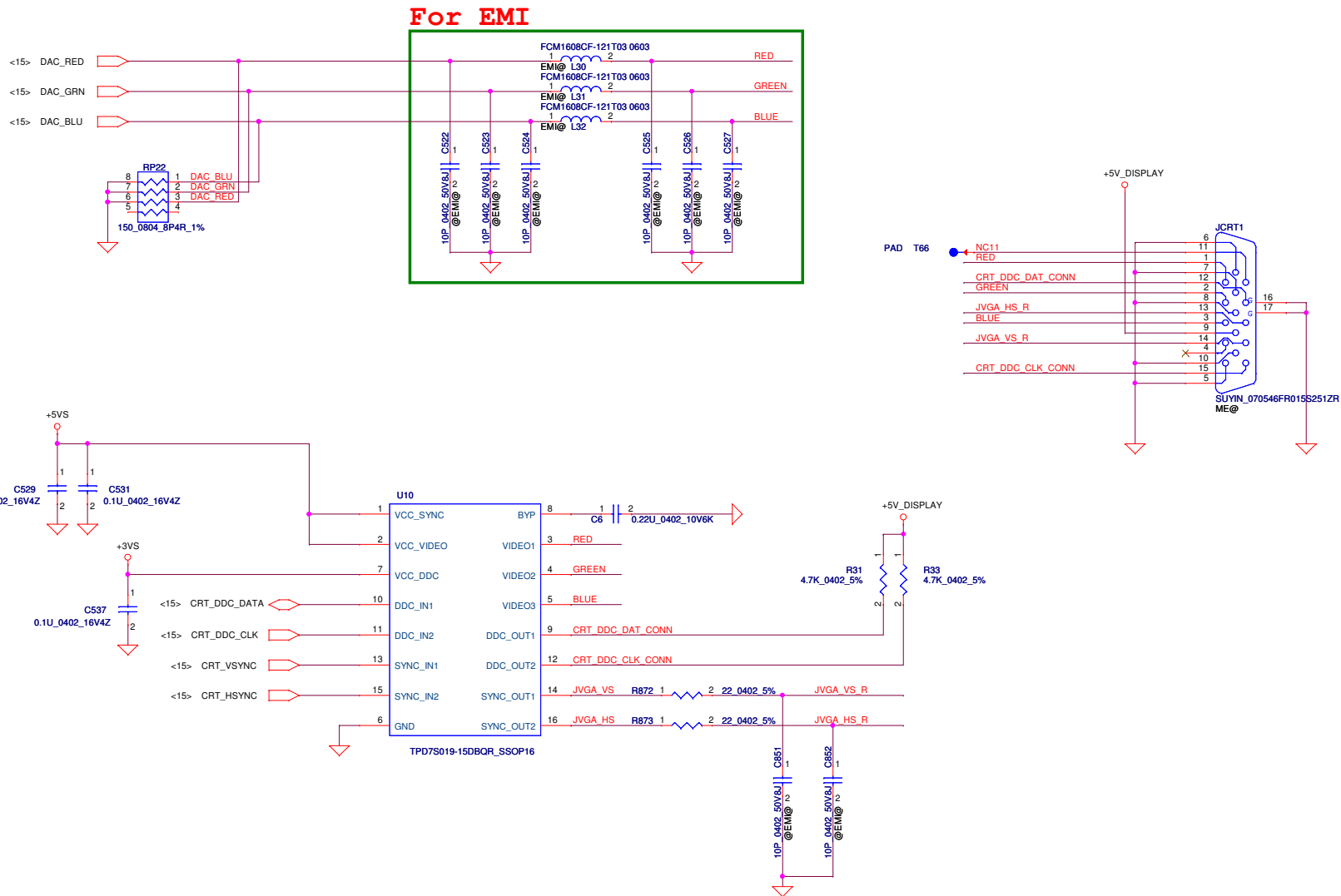
VGA LCD/PANEL BD. Conn.



For EMI

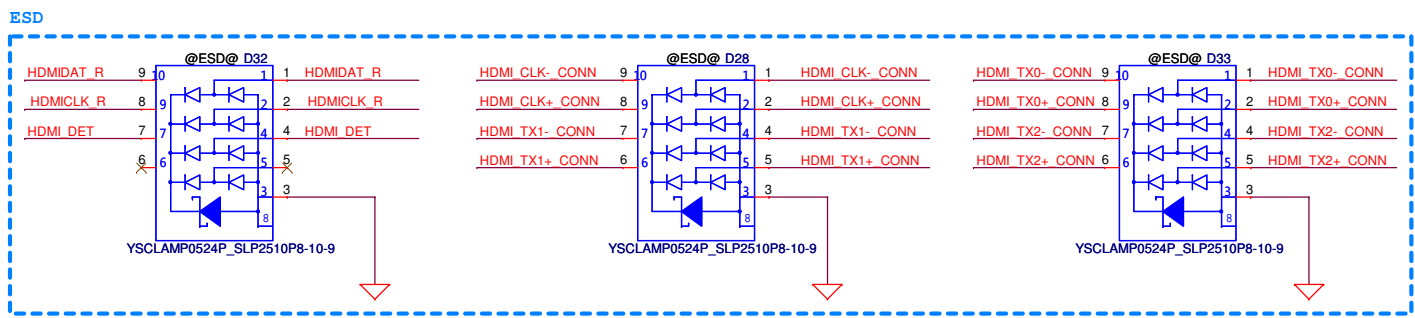
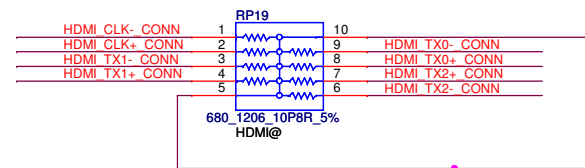
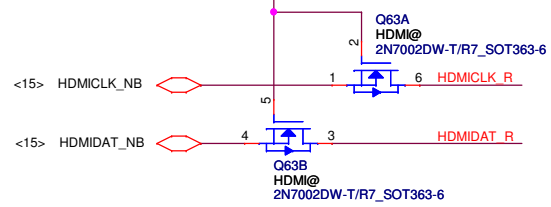
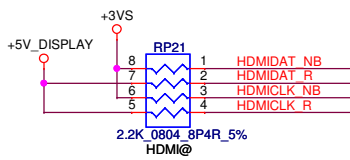
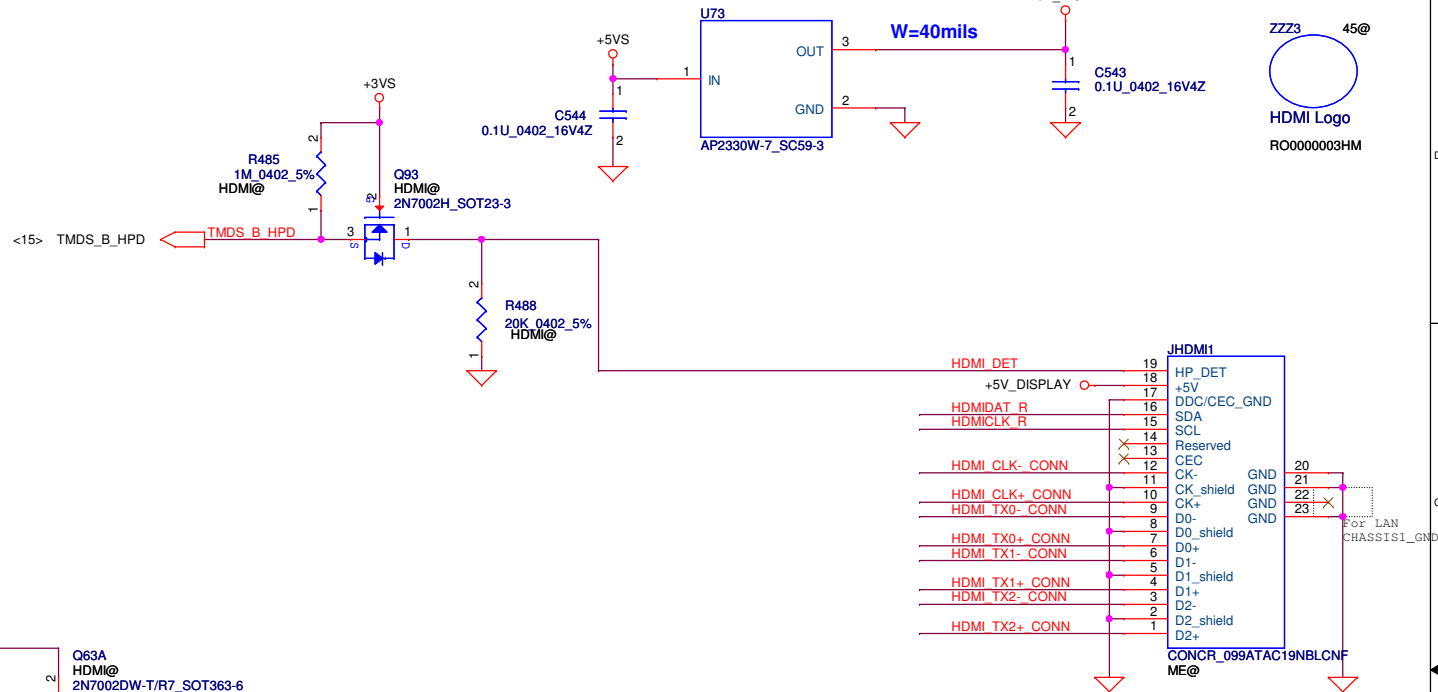
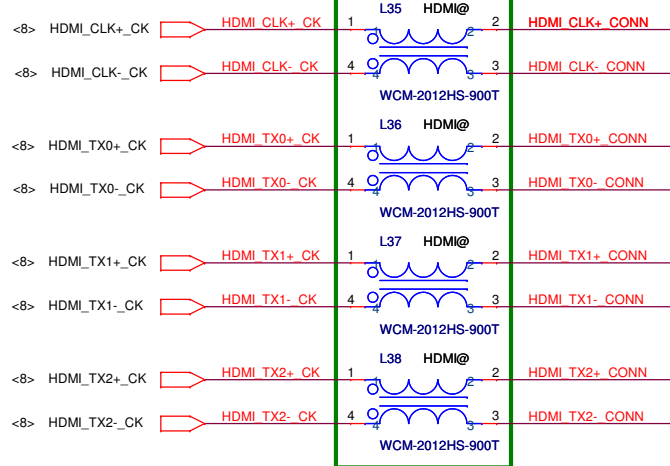


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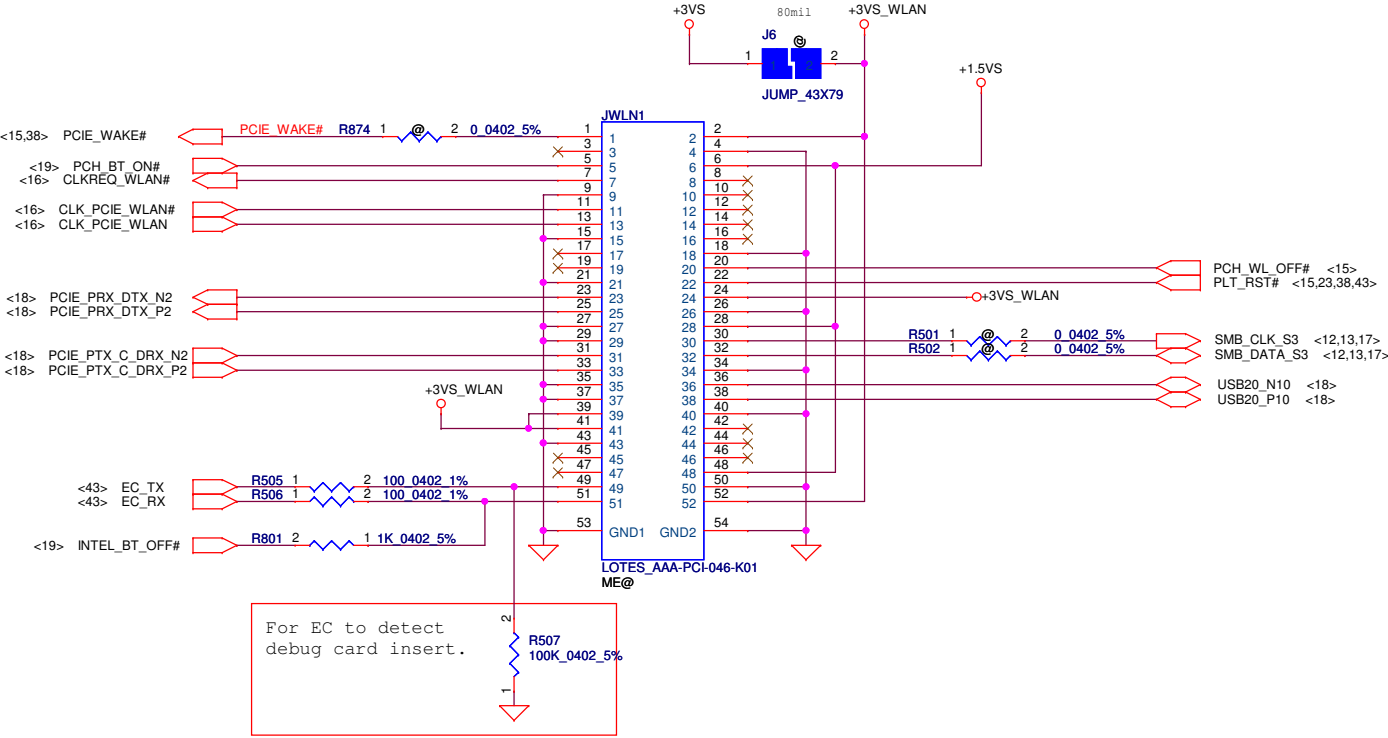
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For EMI



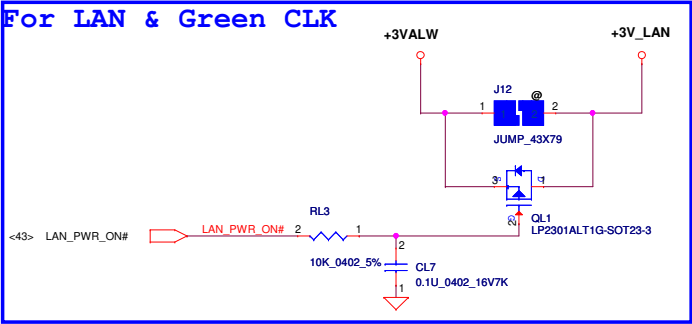
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2015/01/15				Title				HDMI CONN			
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Mini-Express Card for WLAN/WiMAX(Half)

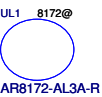
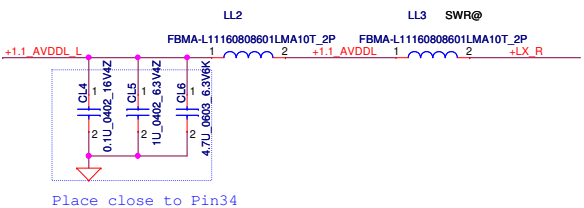
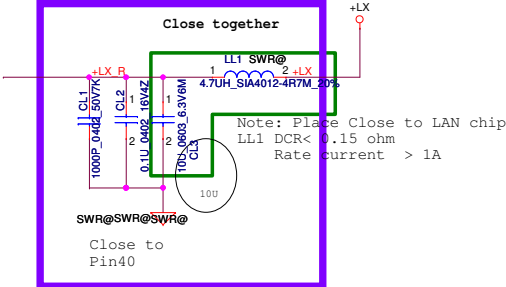
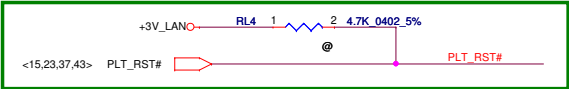


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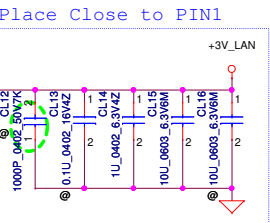
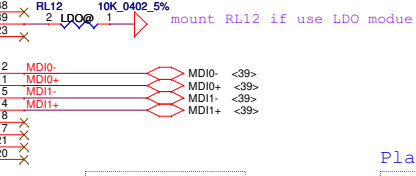
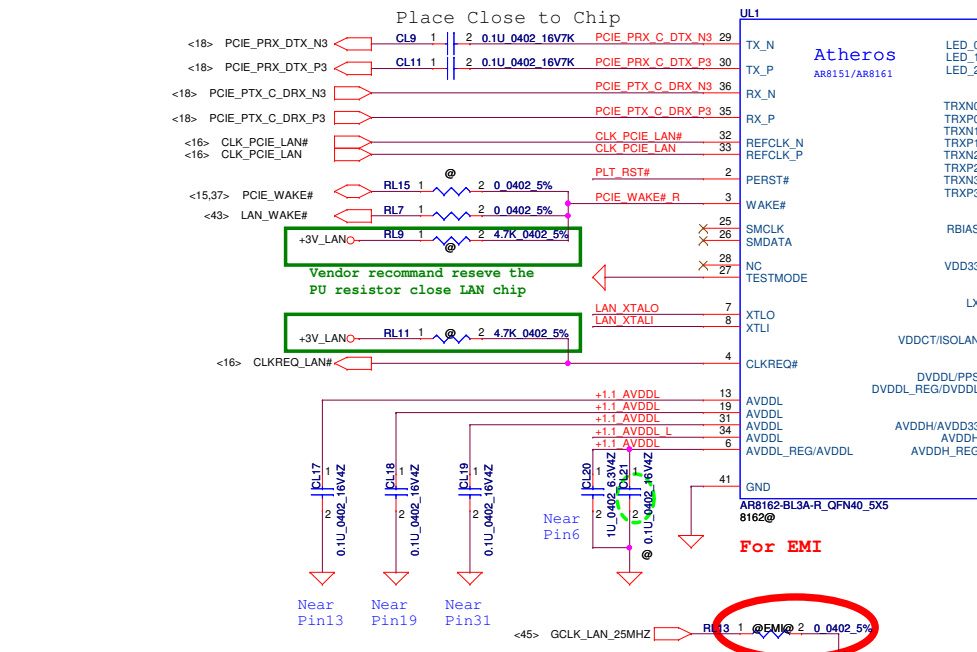
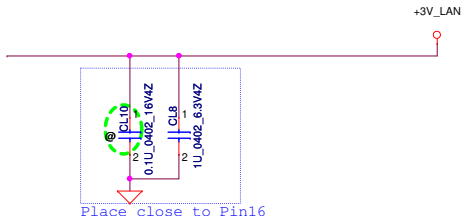
For LAN & Green CLK



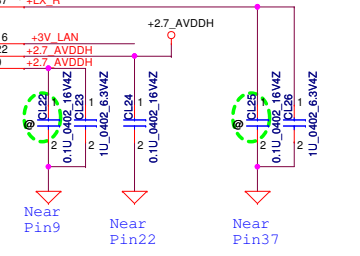
Vendor recommend reseve the PU resistor close LAN chip



Pin	Configure signal	Description
LED[1]	Regulator select	1 Switch mode regulator(SWR) mode 0 Linear regulator (LDO) mode *



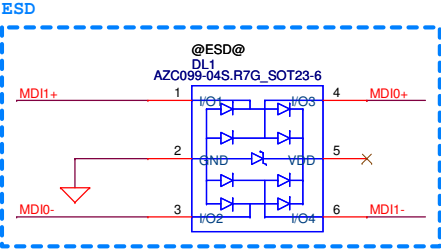
don't @ (could be B C cost done)



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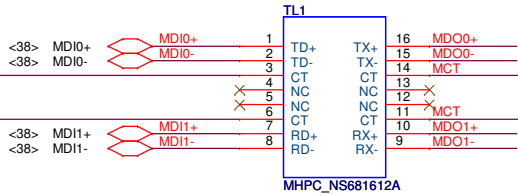
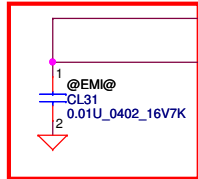
DL1
1'S PN:SC300001G00
2'S PN:SC300002E00

Place Close to TL1

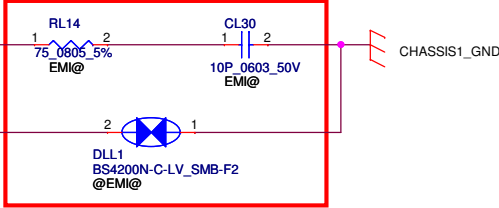


Reserve gas tube for EMI go rural solution

For EMI

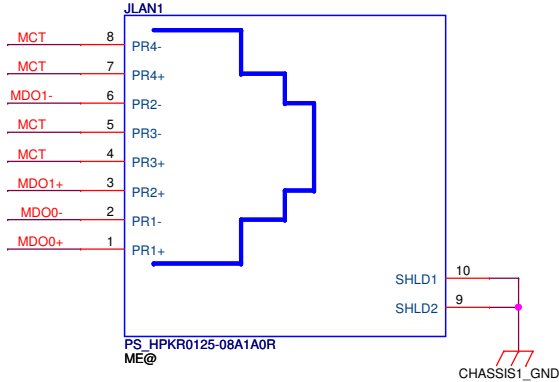
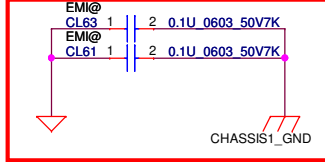


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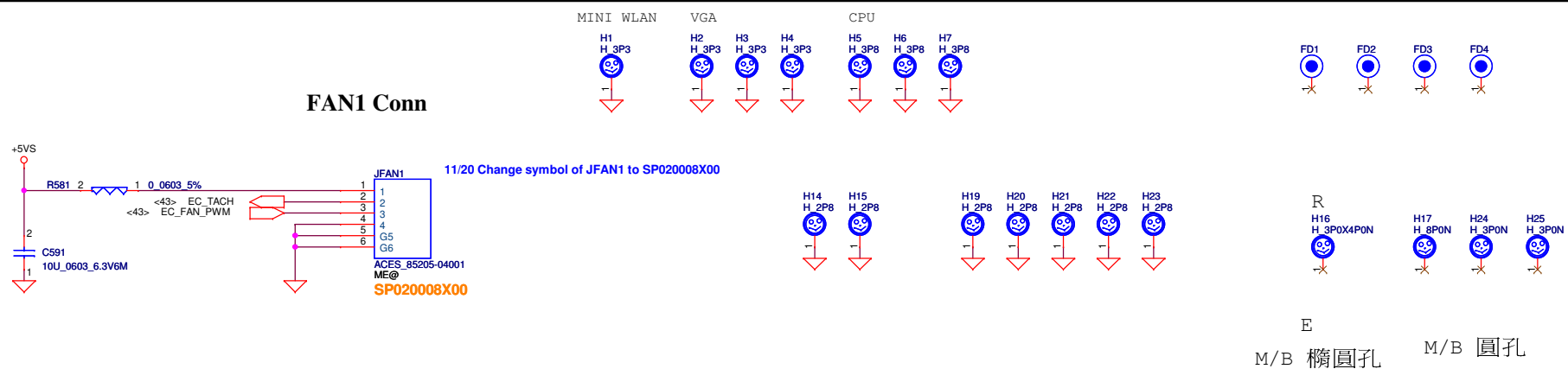
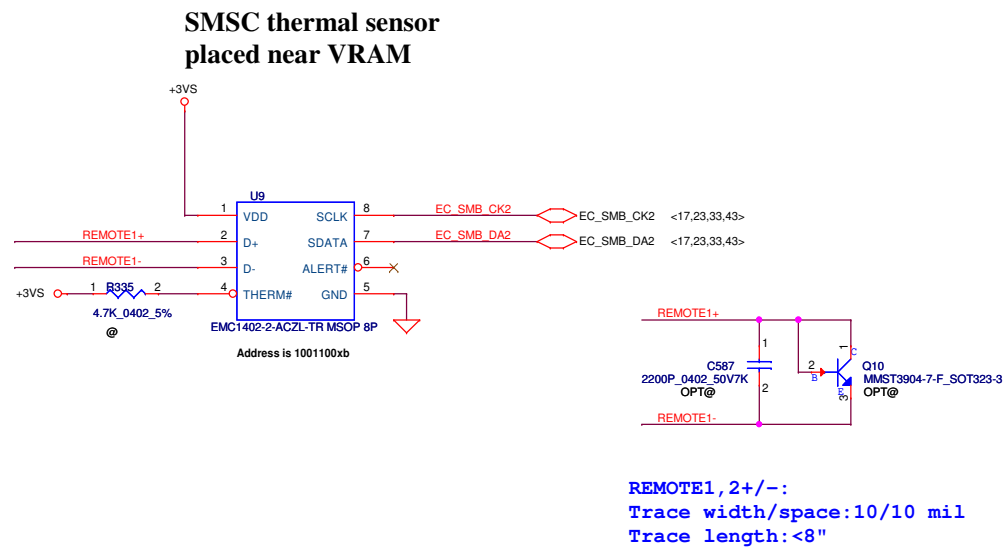


Place Close to TL1

For EMI

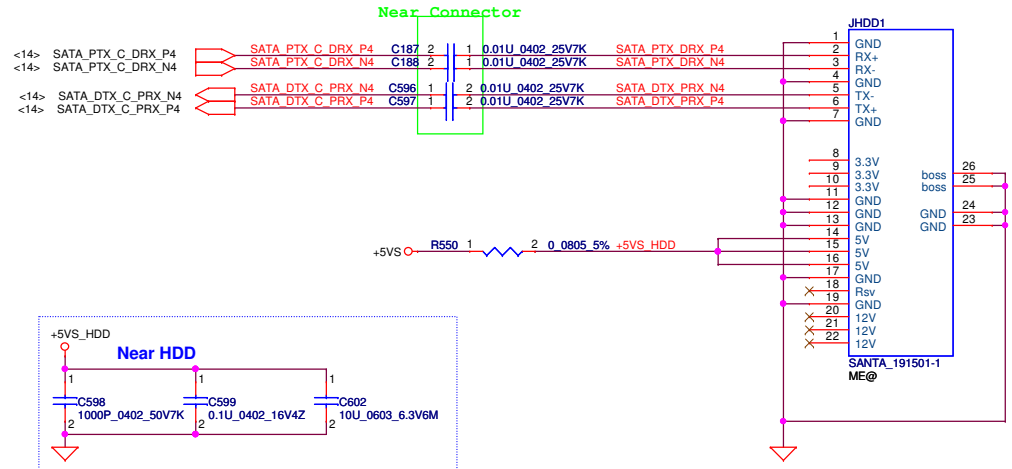


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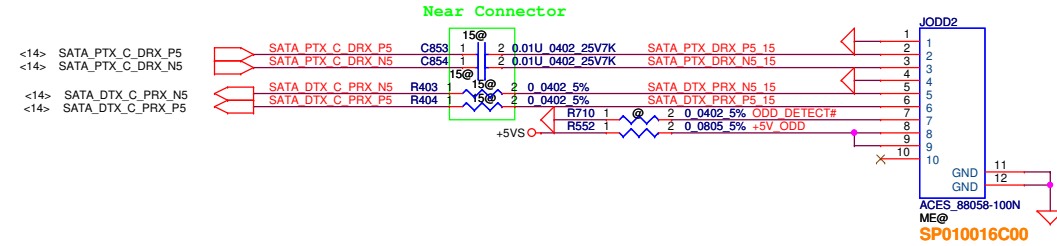


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SATA HDD Conn.



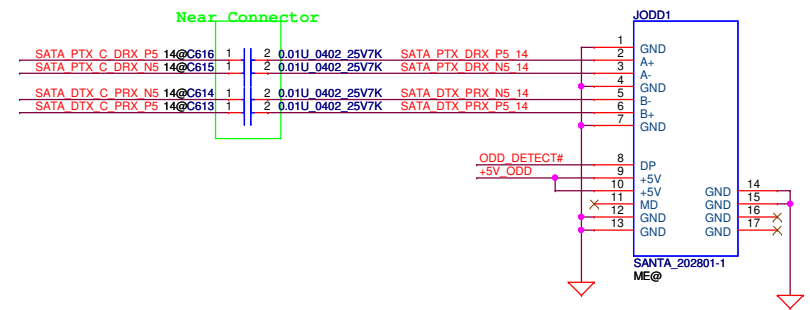
FOR 15" SATA ODD FFC Conn.



11/20 Change symbol of JODD2 to SP010016C00

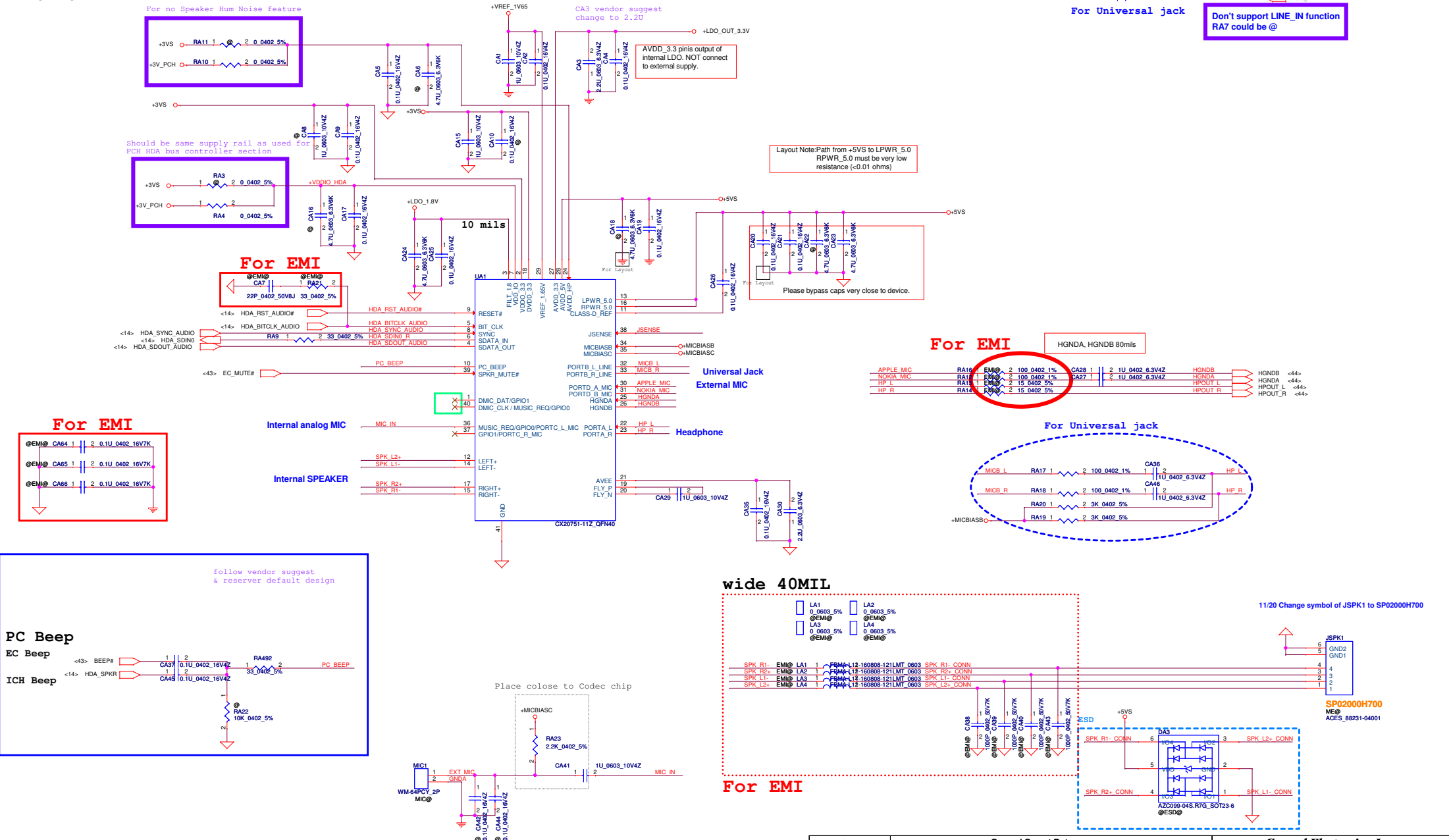
Co-lay

FOR 14" SATA ODD Conn.

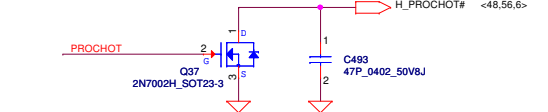
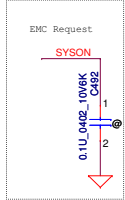
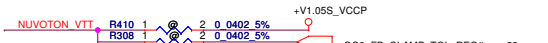
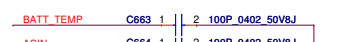
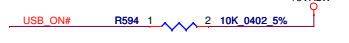
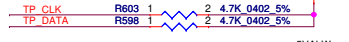
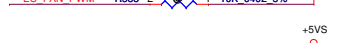
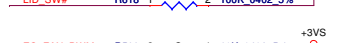
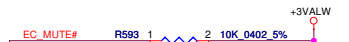
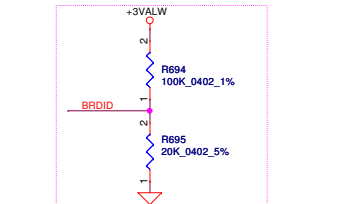
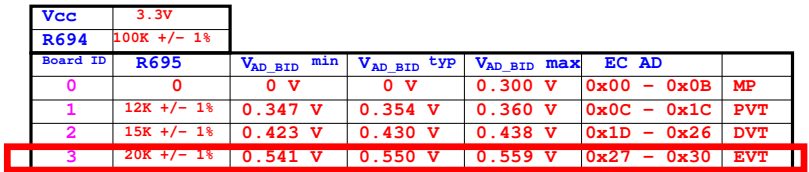


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CX20757
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

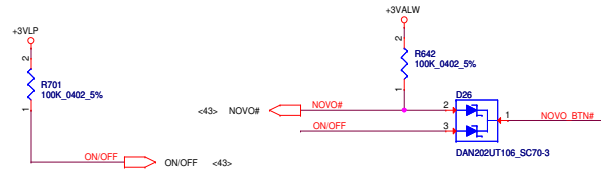


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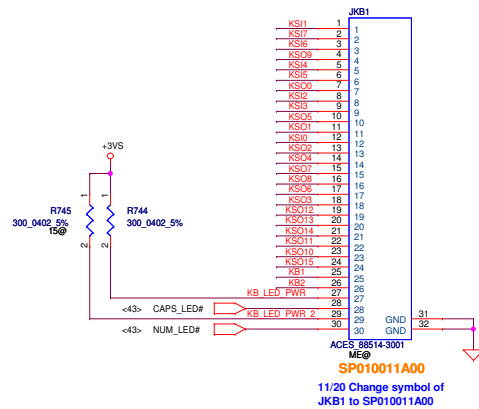
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								BIOS & EC I/O Port			
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								LA-A191P		0.1	
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PWR Button For Debug

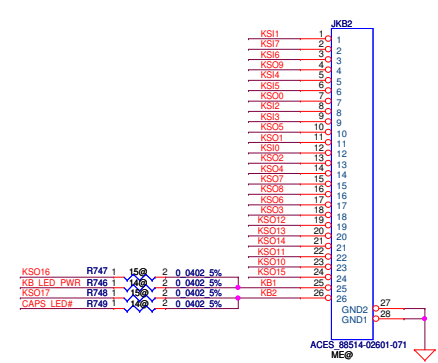


Key Board Conn.

For 15"



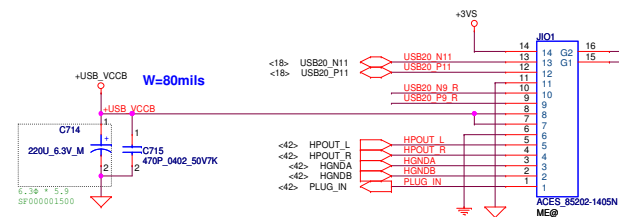
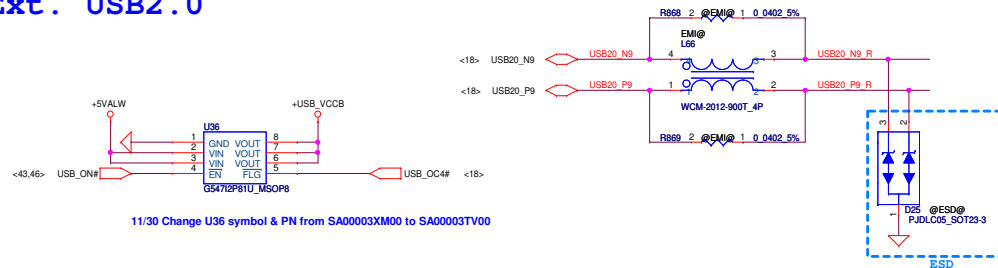
For 14"



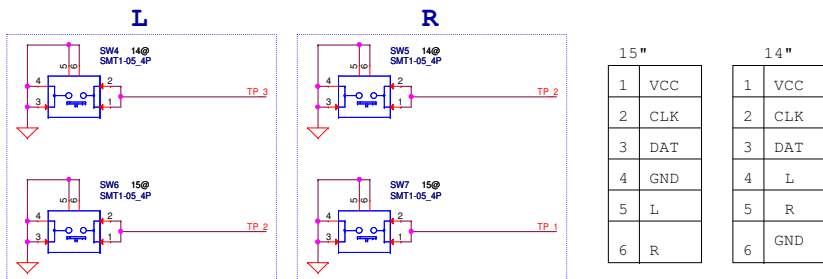
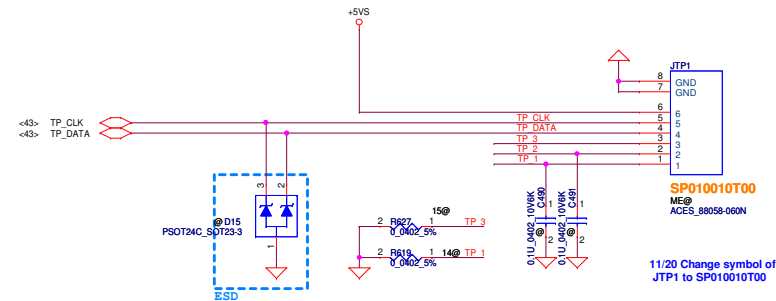
IO/B Conn.

Ext. USB2.0

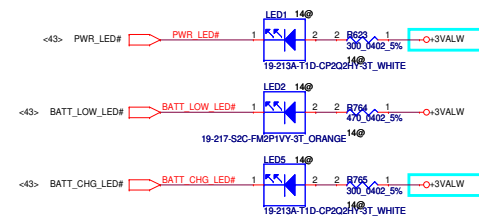
For EMI



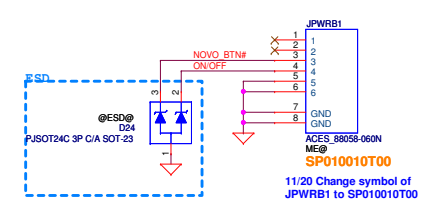
TP Switch & TP Conn.



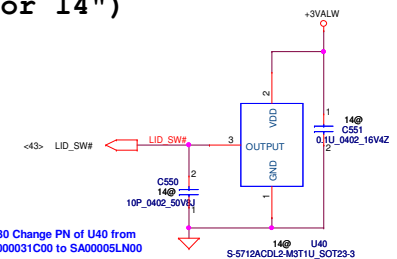
LED



PWR/B Conn.

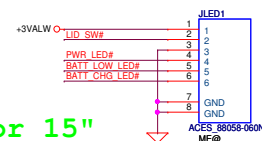


Lid SW(For 14")



LED/B Conn.

For 15"



U71 GCLK244@



SLG3NB244VTR_TQFN16_2X3

For GreenCLK generate CLK:
Mount: All parts in this page except
Swing Level RES (Marked "")**
NA: PD108,
Y1,R98,C180,C181,
Y2,R169,C196,C197,
Y6,C968,C969

Close to GCLK

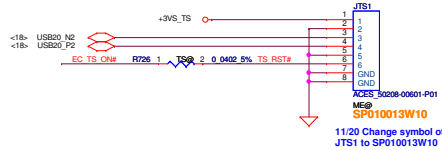
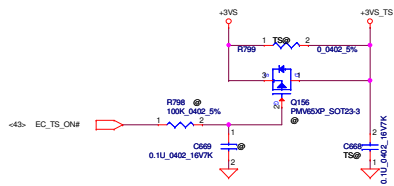
```
PCH_32.768K
NV_GPU
LAN
PCH_25M
```

**Reserved for Swing Level adjustment
(Close GCLK side)**

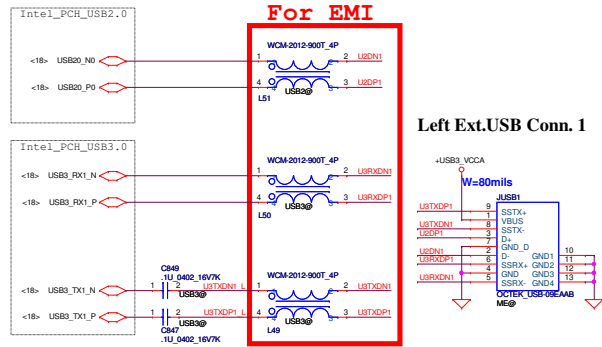
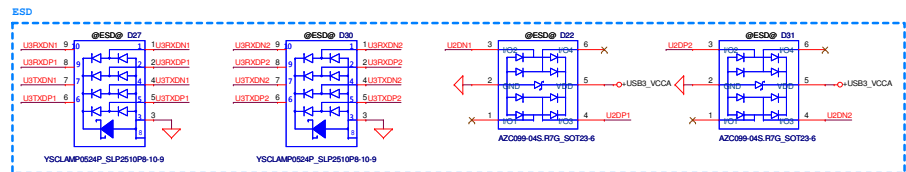
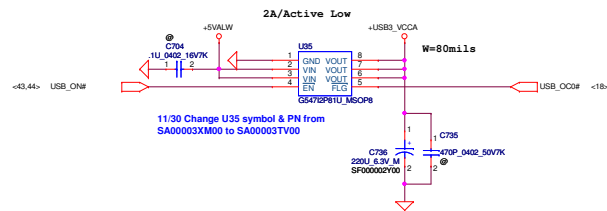
For EMI

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				LA-A191P		
				Date:	Wednesday, January 16, 2013	Sheet 45 of 59

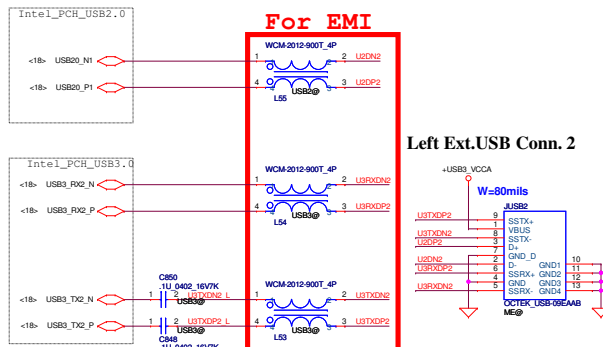
Touch Screen



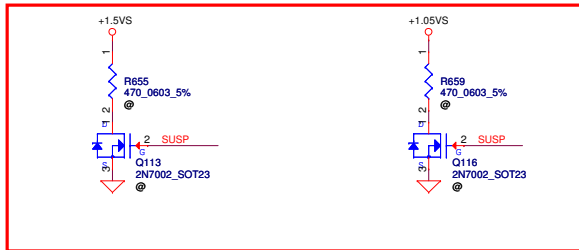
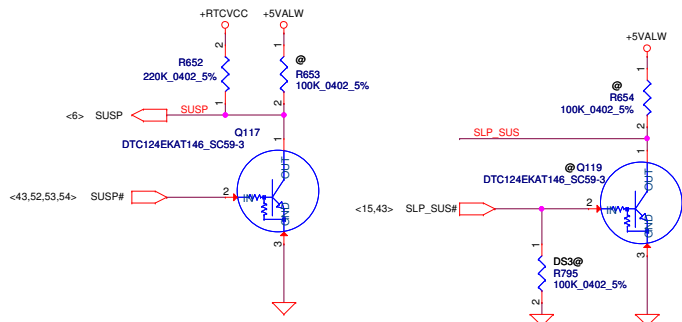
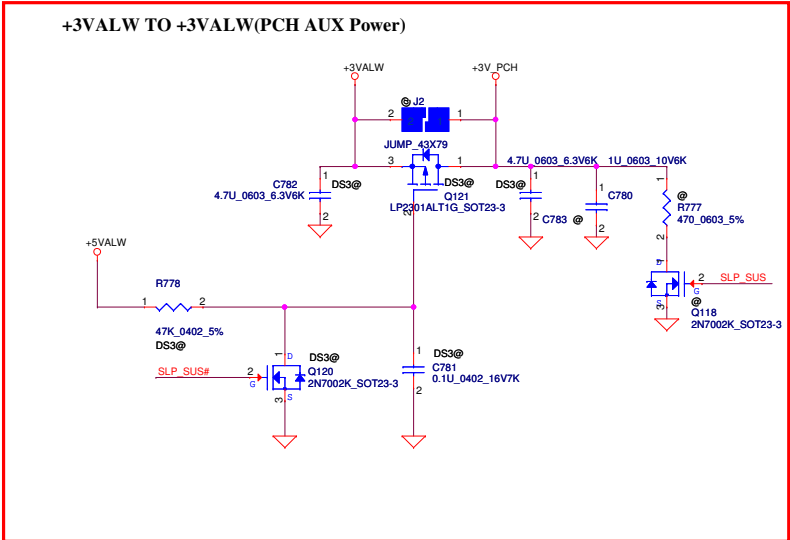
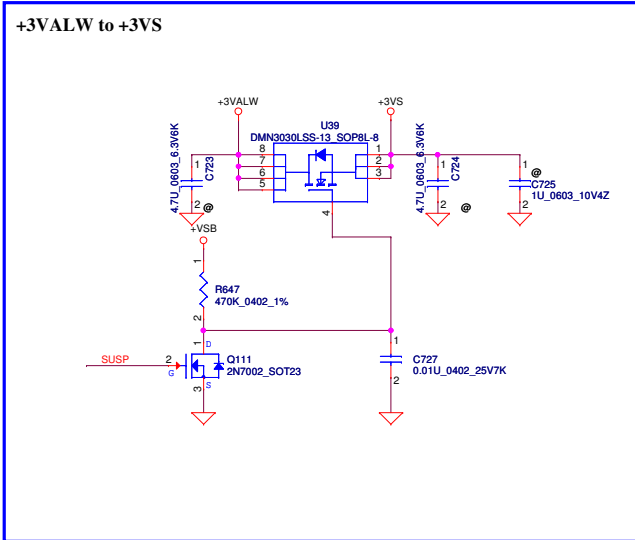
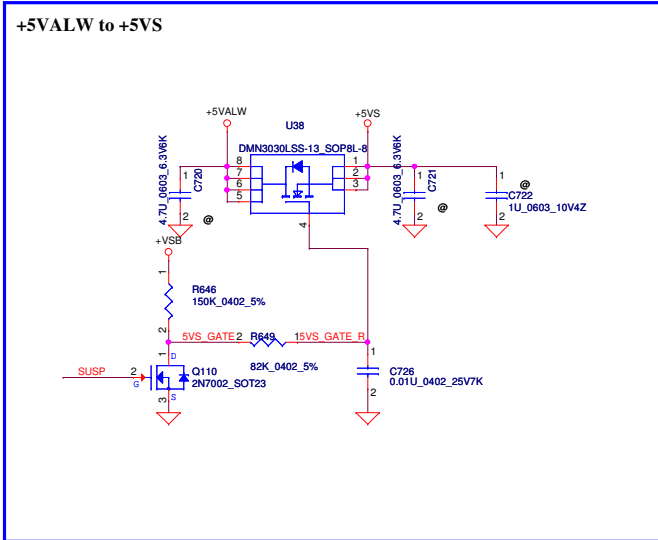
USB3.0



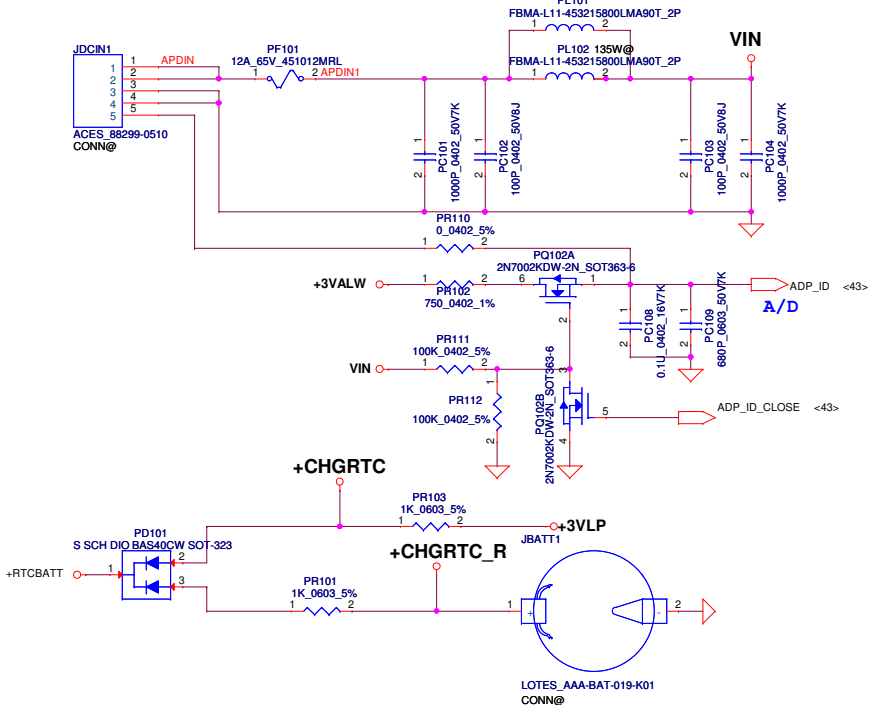
Place TX AC coupling Cap (C843~C850). Close to connector



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Document Number	LA-A191P	Rev 0.1
Date	Wednesday, January 16, 2013	Sheet 46 of 69

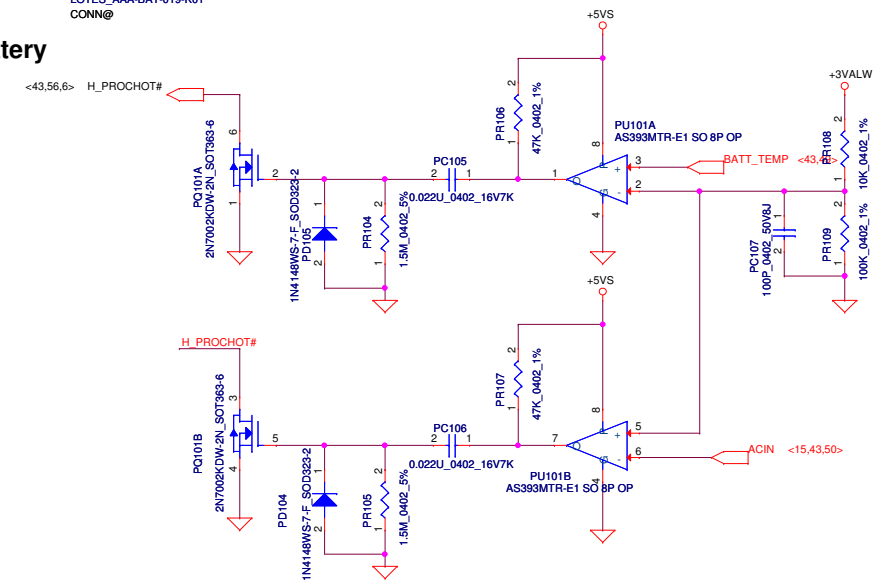


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Size	Custom	Document Number	LA-A191P	Rev	0.1
Date:	Wednesday, January 16, 2013	Sheet	47	of	59

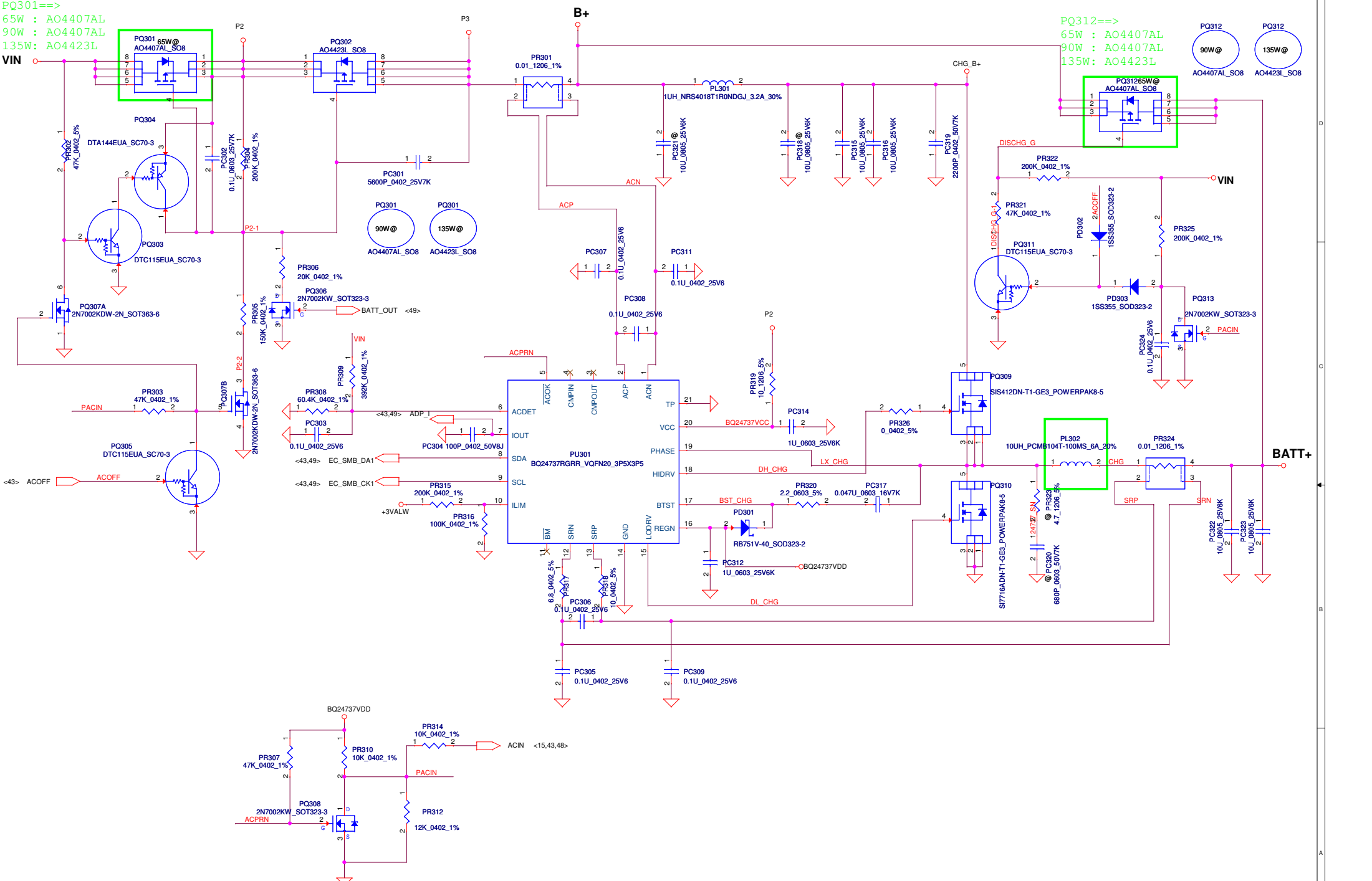


ADP_ID		
AC Adapter	90W	65W
R(K ohm)	open	10
ADP_ID(V)	3.3	1.65
Detection voltage	>2.64	1.32~1.98

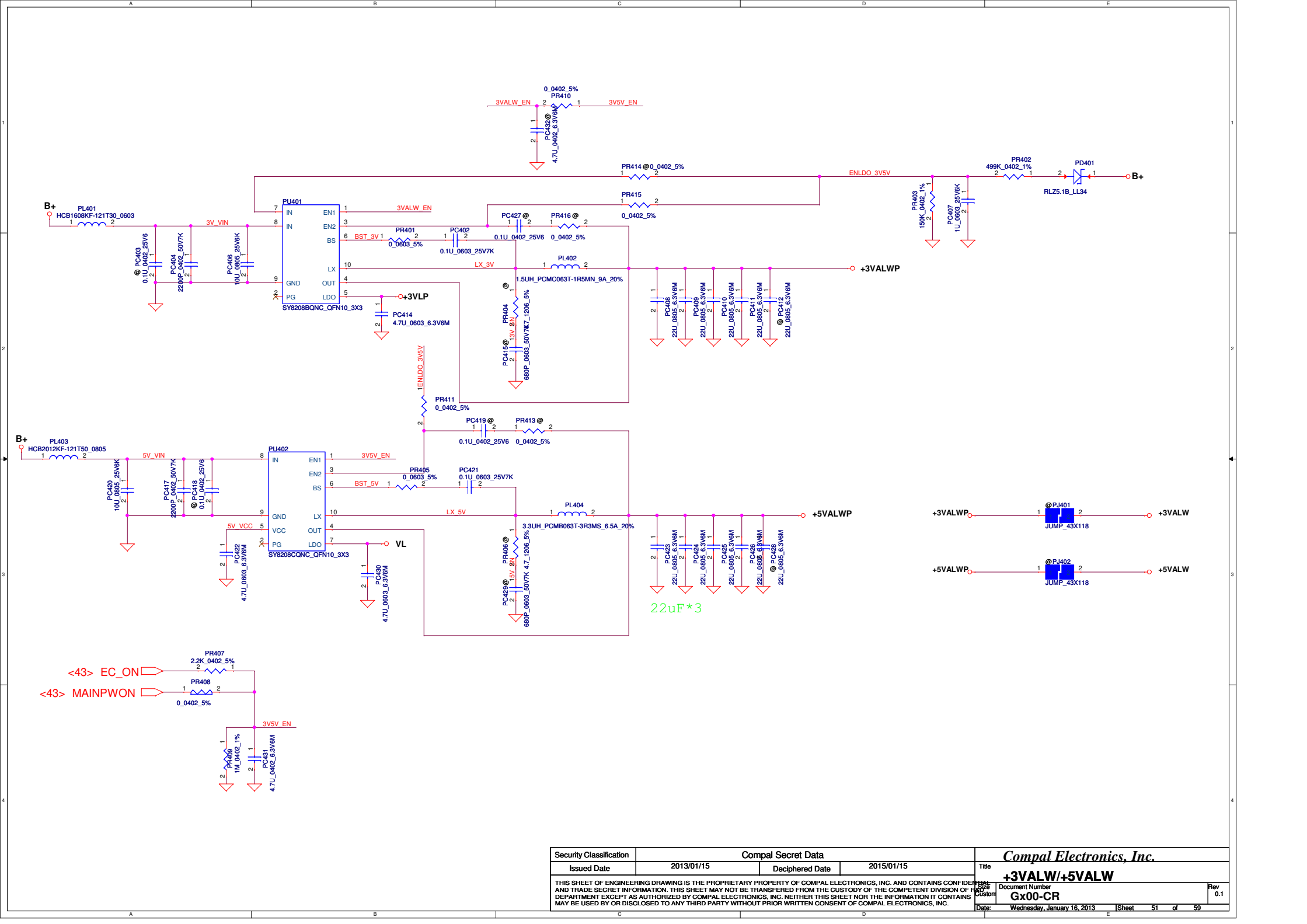
RTC Battery



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				Gx00
				Rev
				0.1
				Date: Wednesday, January 16, 2013
				Sheet 48 of 59

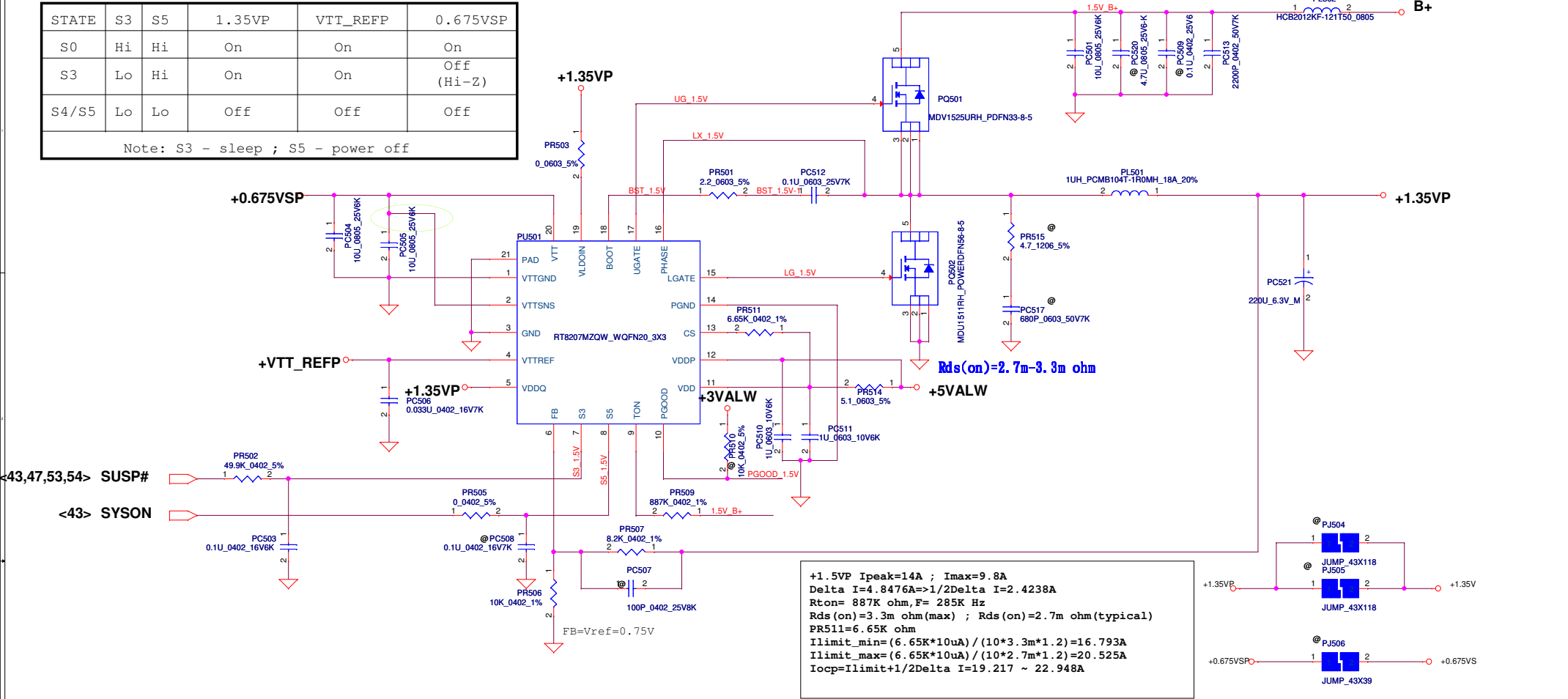


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2013/01/15		Deciphered Date		2015/01/15		Title	
										CHARGER	
										Gx00-CR	
										Rev 0.1	
										Date: Wednesday, January 16, 2013	
										Sheet 50 of 59	

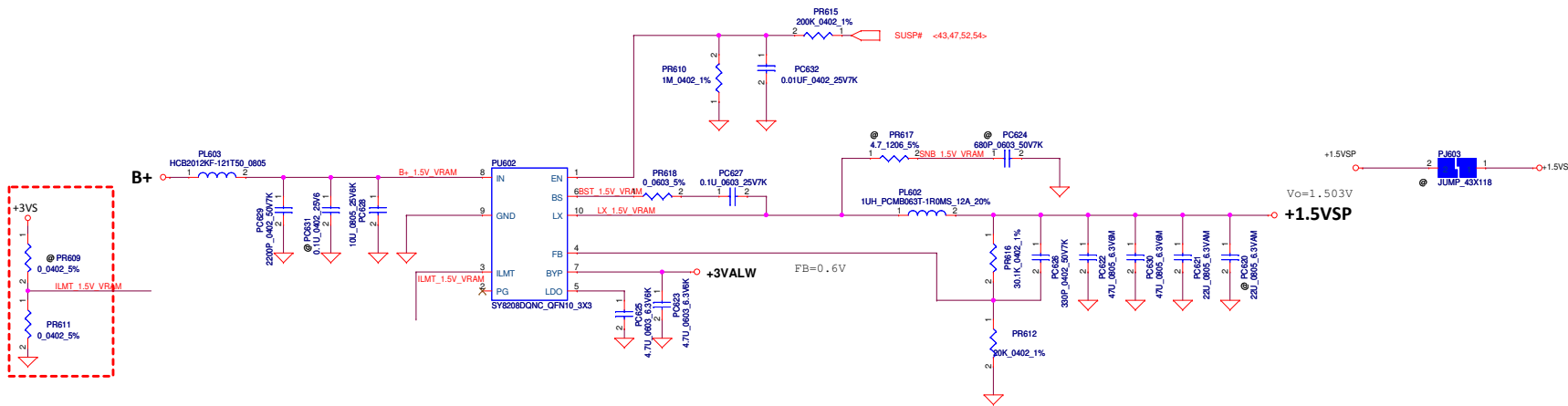


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STATE	S3	S5	1.35VP	VTT_REFP	0.675VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					

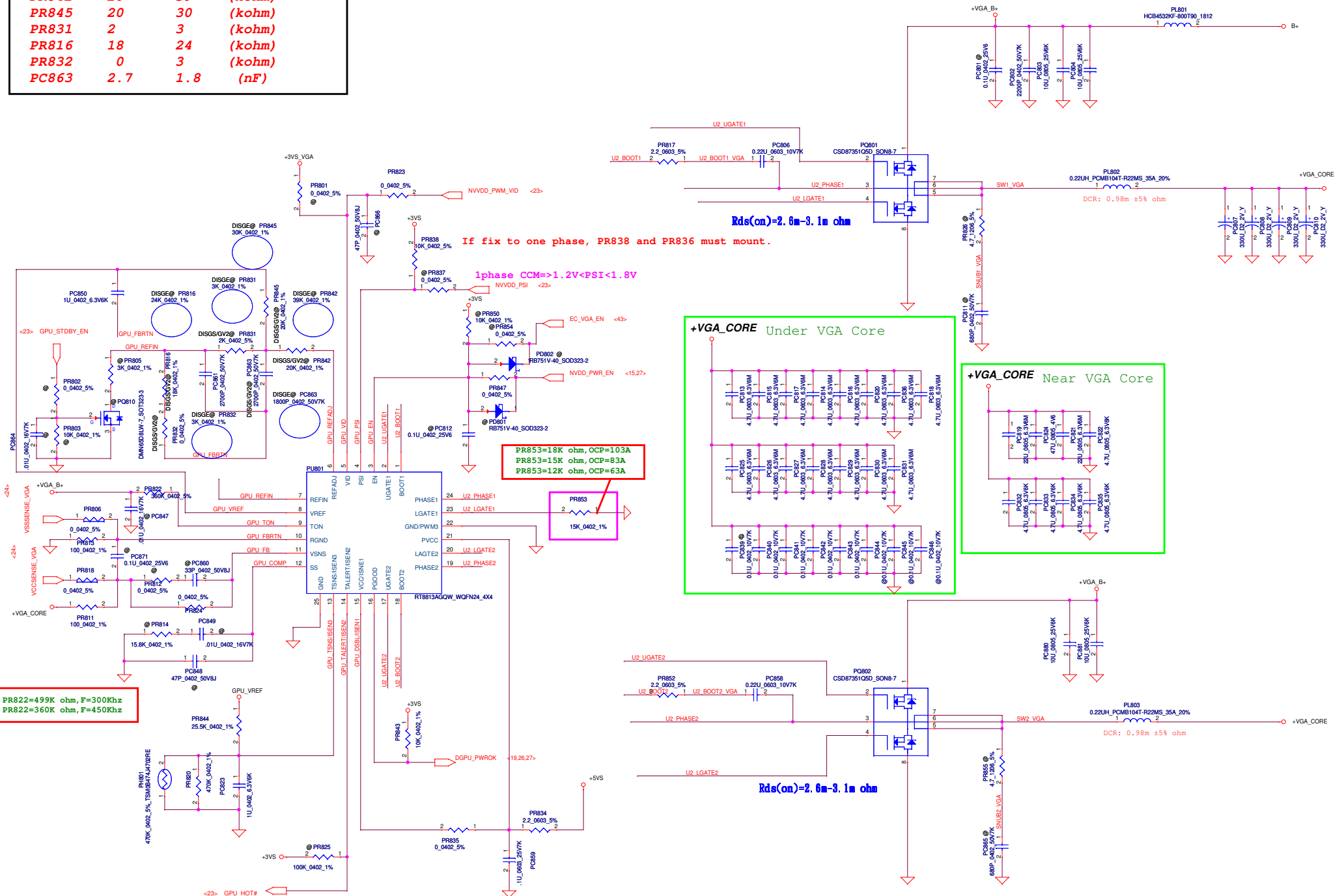


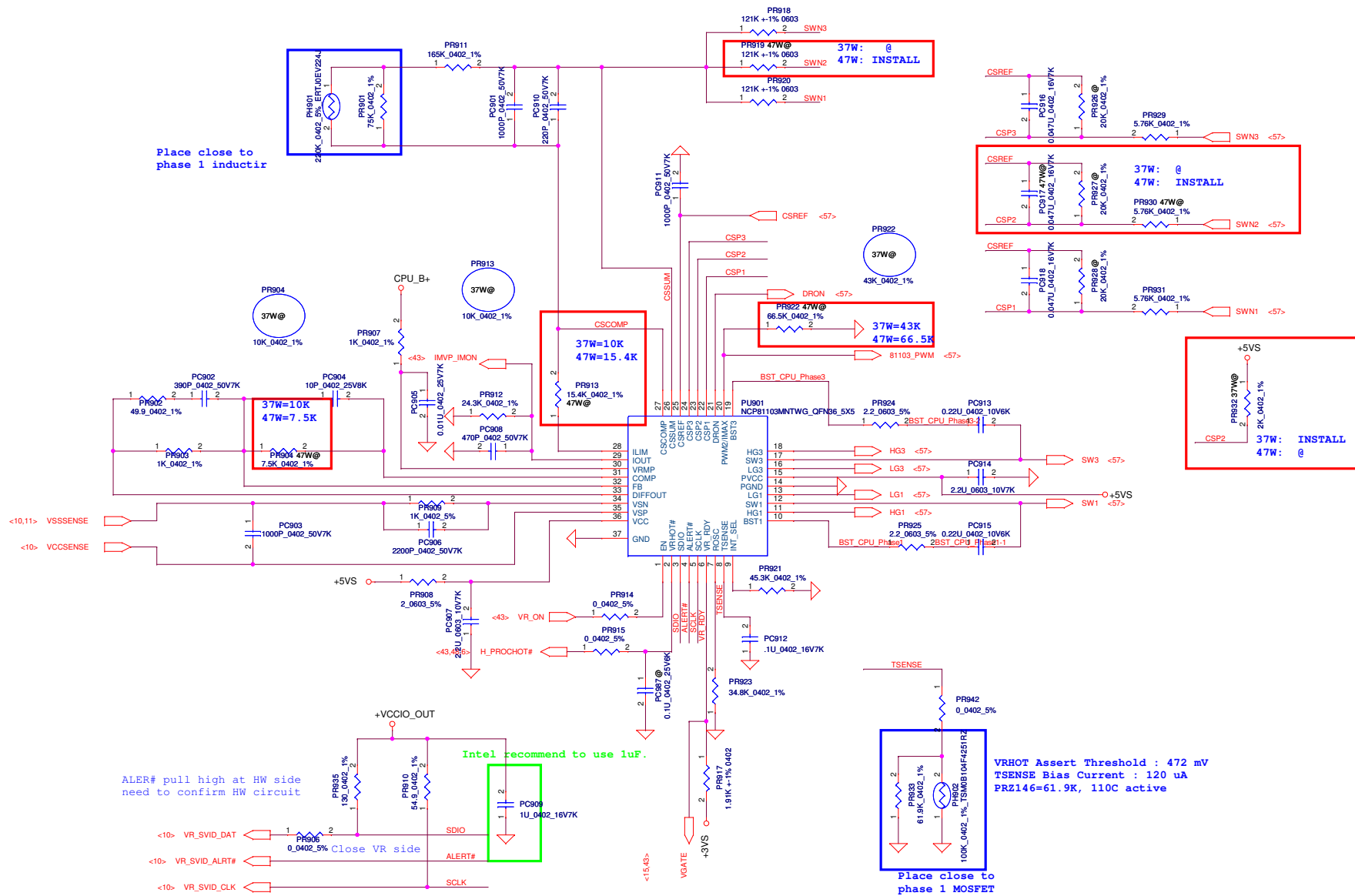
+1.5VP Ipeak=14A ; Imax=9.8A
Delta I=4.8476A=>1/2Delta I=2.4238A
Rton= 887K ohm,F= 285K Hz
Rds(on)=3.3m ohm(max) ; Rds(on)=2.7m ohm(typical)
PR511=6.65K ohm
Ilimit_min=(6.65K*10uA)/(10*3.3m*1.2)=16.793A
Ilimit_max=(6.65K*10uA)/(10*2.7m*1.2)=20.525A
Iocp=Ilimit+1/2Delta I=19.217 ~ 22.948A

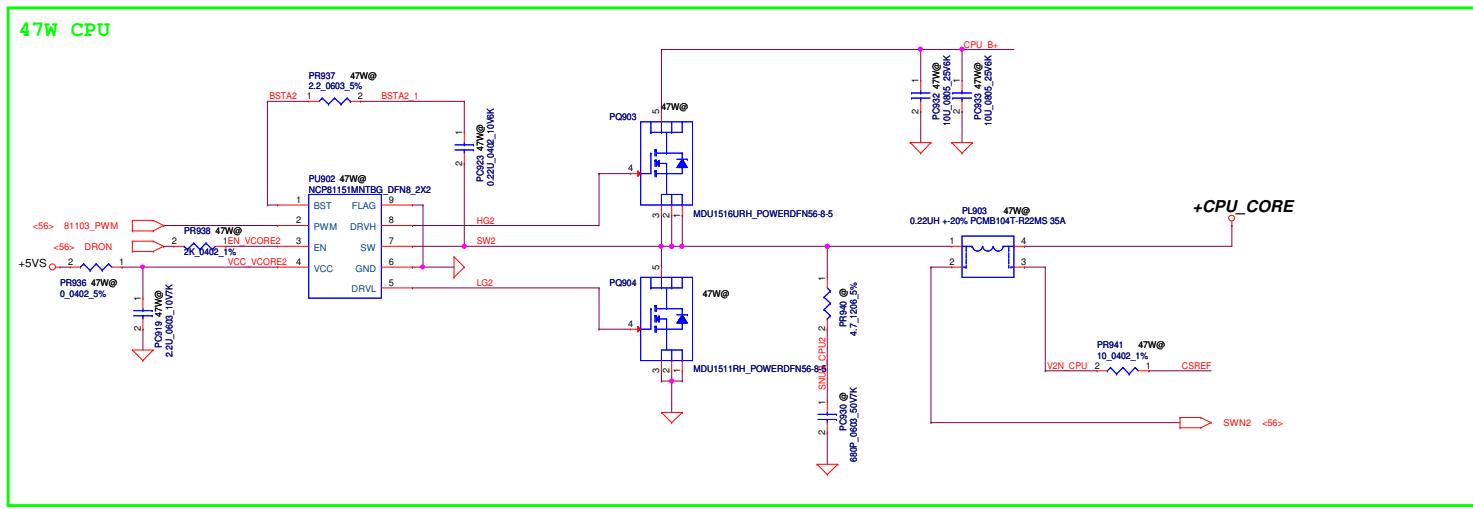
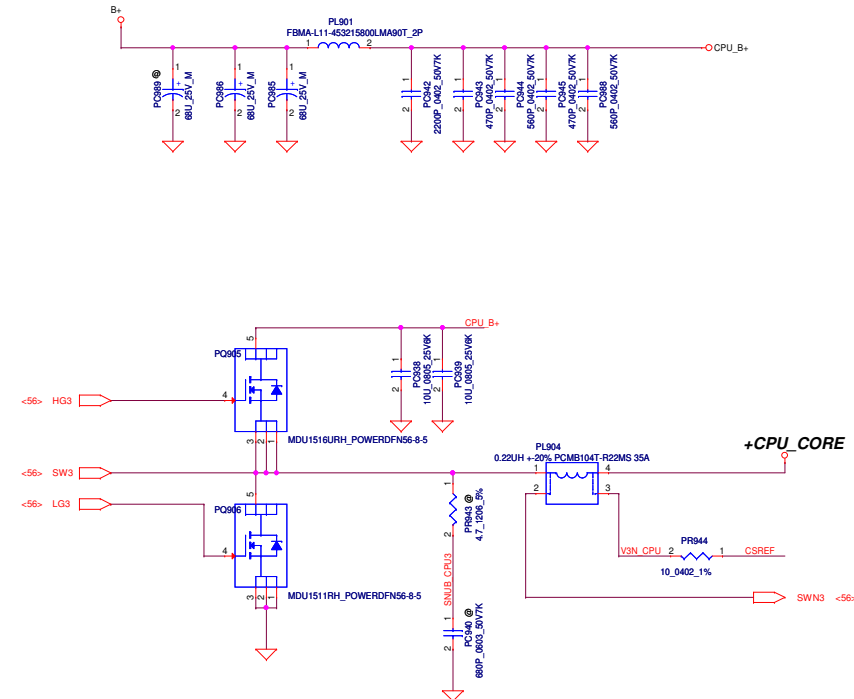
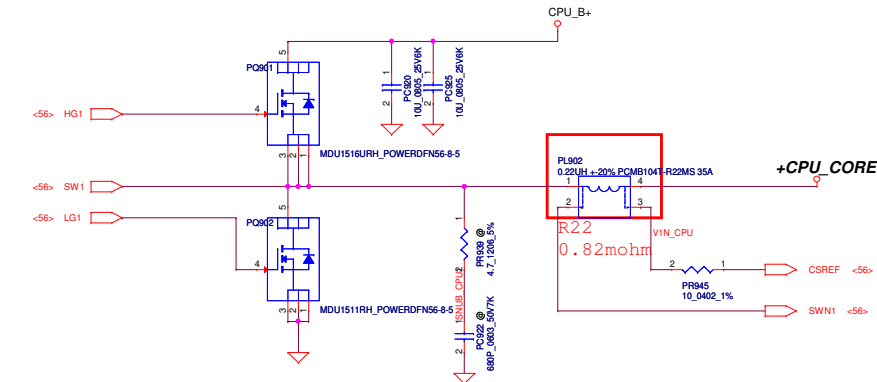


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	GS/GV2	GE	
PR842	20	39	(kohm)
PR845	20	30	(kohm)
PR831	2	3	(kohm)
PR816	18	24	(kohm)
PR832	0	3	(kohm)
PC863	2.7	1.8	(nF)







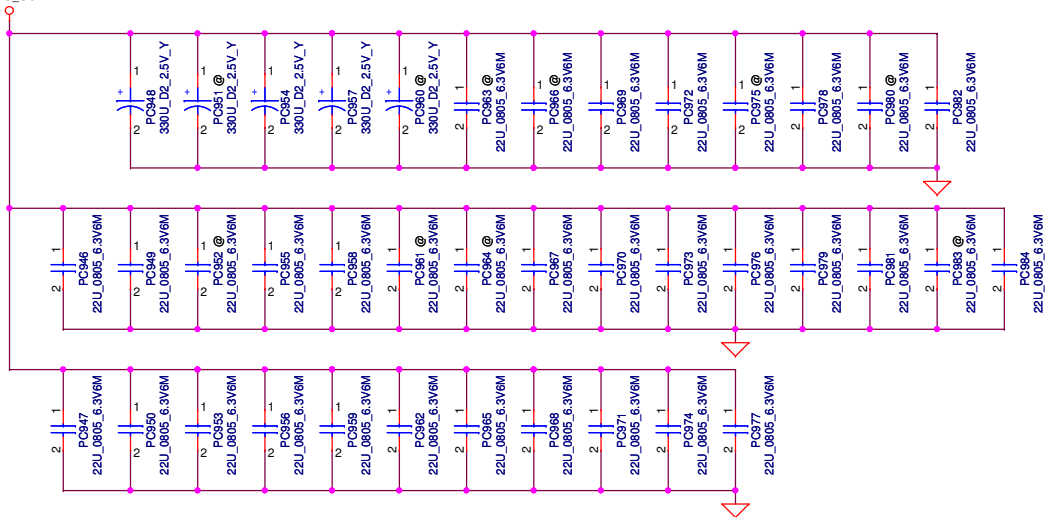
QC 47W CPU
VID1=1.8V
VID2=1.7V
VID3=1.6V
Vboot=1.7V
IccMax=85A
Icc_TDC(PL2)=33A
Icc_TDC(PL1)=27A
Icc_Dyn=60A

DC 37W CPU
VID1=1.8V
VID2=1.7V
VID3=1.6V
Vboot=1.7V
IccMax=55A
Icc_TDC(PL2)=26A
Icc_TDC(PL1)=21A
Icc_Dyn=35A

+CPU_CORE

3 X 330u/9m (47W) 2X330u/9m (37W)
34 X 22u/0805 34 X 22u/0805

+CPU_CORE



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Item	Reason for change	PG#	Modify List	Date	Phase
1	Design Change of IC Package.	50	Change PU401 to SA000061M00(S IC SY8208BQNC QFN 10P PWM)	2012/11/22	DVT
2	Design Change of IC Package.	50	Change PU402 to SA000061N00(S IC SY8208CQNC QFN 10P PWM)	2012/11/22	DVT
3	Design Change of IC Package.	52	Change PU602 to SA000061Q00(S IC SY8208DQNC QFN 10P PWM)	2012/11/22	DVT
4	Add ADP_ID Circuit.	47	Add PQ102 to SB00000EO10(S TR 2N7002KDW 2N SOT-363-6 PANJIT) Add PR111,PR112 to SD028100380(S RES 1/16W 100K +-5% 0402)	2012/12/03	DVT
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					